PHILIPS

Data handbook

Electronic components and materials

Semiconductors and integrated circuits

Part 5 July 1973

Linear Integrated Circuits

SEMICONDUCTORS AND INTEGRATED CIRCUITS

Part 5 **July 1973**

General

Linear integrated circuits

Index and maintenance type list at the back

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DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, subassemblies and materials; it is made up of three series of handbooks each comprising several parts.

ELECTRON TUBES	**BLUE**
SEMICONDUCTORS AND INTEGRATED CIRCUITS	**RED**
COMPONENTS AND MATERIALS	**GREEN**

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

If you need confirmation that the published data about any of our products are the latest available, please contact our representative. He is at your service and will be glad to answer your inquiries.

December 1972

ELECTRON TUBES (BLUE SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1a **Transmitting tubes for communications** **April 1973**
and Tubes for r.f. heating **Types PB2/500 ÷ TBW15/125**

Part 1b **Transmitting tubes for communication** **May 1973**
Tubes for r.f. heating
Amplifier circuit assemblies

Part 2 **Tubes for microwave equipment** **February 1972**

Part 3 **Special Quality tubes;** **March 1972**
Miscellaneous devices

Part 4 **Receiving tubes** **June 1972**

Part 5 **Cathode-ray tubes; Camera tubes** **July 1972**

Part 6 **Products for nuclear technology** **September 1972**
Photodiodes

Photomultiplier tubes
Channel electron multipliers
Scintillators
Photoscintillators
Radiation counter tubes
Semiconductor radiation detectors
Neutron generator tubes
Photo diodes

Part 7 **Gas-filled tubes** **October 1972**

Voltage stabilizing and reference tubes
Counter, selector, and indicator tubes
Trigger tubes
Switching diodes
Thyratrons
Ignitrons
Industrial rectifying tubes
High-voltage rectifying tubes

Part 8 **T.V. Picture tubes** **November 1972**

SEMICONDUCTORS AND INTEGRATED CIRCUITS (RED SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1a Rectifier diodes and thyristors — **December 1972**

Rectifier diodes
Voltage regulator diodes
Transient suppressor diodes
Thyristors diacs, triacs
Ignistors
Rectifier stacks

Part 1b Diodes — **December 1972**

Small signal germanium diodes
Small signal silicon diodes
Special diodes
Voltage regulator diodes
Voltage reference diodes
Tuner diodes

Part 2 Low frequency and deflection transistors — **January 1973**

Part 3 High frequency and switching transistors — **February 1973**

Part 4a Special semiconductors — **March 1973**

Transmitting transistors
Microwave devices
Field effect transistors
Dual transistors
Microminiature devices for thick- and thin-film circuits

Part 4b Devices for opto-electronics — **March 1973**

Photosensitive diodes and transistors
Light emitting diodes
Infra-red sensitive devices
Photocouplers
Photoconductive devices

Part 5 Linear integrated circuits — **July 1973**

Part 6 Digital integrated circuits — **March 1972**

DTL (FC family)
DTL/HNIL (FZ family)
TTL (FJ family)
TTL (GJ family)
CML (GH family)
MOS (FD family)

COMPONENTS AND MATERIALS (GREEN SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1 Circuit Blocks, Input/Output Devices, Electro-mechanical Components, Peripheral Devices — **January 1973**

Circuit blocks 40-Series and CSA70
Counter modules 50-Series
Norbits 60-Series, 61- Series
Circuit blocks 90-Series
Input/output devices
Electro-mechanical components
Peripheral devices

Part 2 Resistors, Capacitors — **April 1973**

Electrolytic capacitors
Paper capacitors and film capacitors
Ceramic capacitors
Variable capacitors
Fixed resistors
Variable resistors
Non-linear resistors
(VDR, LDR, NTC, PTC)

Part 3 Radio, Audio, Television — **June 1973**

FM tuners
Loudspeakers
Television tuners, aerial input assemblies
Components for black and white television
Components for colour television
Deflection assemblies for camera tubes

Part 4 Magnetic Materials, Piezoelectric Ceramics, Ni Cd cells — **May 1972**

Ferrites for radio, audio and television
Small coils and assembling parts
Ferroxcube potcores and square cores
Ferroxcube transformer cores
Piezoelectric ceramics
Permanent magnet materials
Cylindrical nickel cadmium cells *)

Part 5 Memory Products, Magnetic Heads, Quartz Crystals, Microwave Devices, Variable Transformers — **August 1972**

Ferrite memory cores
Matrix planes, matrix stacks
Complete memories
Magnetic heads
Quartz crystal units, crystal filters
Isolators, circulators
Variable mains transformers

Part 6 Electric Motors and Accessories, Timing and Control Devices — **October 1972**

Small synchronous motors
Stepper motors
D.C. motors
D.C. tachogenerators
Asynchronous motors
Indicators for built-in test equipment
Time indicators, timers, timing motors
Aircraft electronic clock system

Part 7 Circuit Blocks — **September 1971**

Circuit blocks 100 kHz Series
Circuit blocks 1-Series
Circuit blocks 10-Series
Circuit blocks for ferrite core memory drive

*) These items have been discontinued

General

PREFACE TO DATA OF INTEGRATED CIRCUITS

1. General

The published data comprise particulars needed by designers of equipment in which integrated circuits are to be incorporated, and criteria on which to base acceptance testing of such circuits. For ease of reference, the data on each circuit are grouped according to the several headings discussed below.
The limiting values quoted under the headings Characteristics and Package Outline may be taken as references for acceptance testing.
Values cited as typical are given for information only.
For an explanation of the type designation code, see the section Type Designation.
For an explanation of the letter symbols used in designating terminals and performance of integrated circuits, and the electrical and logic quantities pertaining to them, see the section Letter Symbols.

2. Quick Reference Data

The main properties of the integrated circuit summarized for quick reference

3. Ratings

Ratings are limits beyond which the serviceability of the integrated circuit may be impaired. The ratings given here are in accordance with the Absolute Maximum System as defined in publication no. 134 of the International Electrical Commission; for further details see item 2 of the section Rating Systems.
If a circuit is used under the conditions set forth in the sections Characteristics and Additional System Design Data, its operation within the ratings is ensured.

4. Circuit diagram

Circuit diagrams and logic symbols are given to illustrate the circuit function. The diagrams show only essential elements, parasitic elements due to the method of manufacture normally being omitted. The manufacturer reserves the right to make minor changes to improve manufacturability.

5. System Design Data and Additional System Design Data

System Design Data normally derived from the Characteristics and based on worst-case assumptions as to temperature, loading and supply voltage, are quoted for the guidance of equipment designers. Supplementary information derived from measurements on large production samples may be given under Additional System Design Data.

6. Application information

Under this heading, practical circuit connections and the resulting performance are described. Care has been taken to ensure the accuracy and completeness of the information given, but no liability therefor is assumed, nor is licence under any patent implied.

7. Characteristics

Characteristics are measurable properties of the integrated circuit described. Under a specific set of test conditions compliance with limit values given under this heading establishes the specified performance of the circuit; this can be used as a criterion for acceptance testing.
Values cited as typical are given for information only and are not subject to any form of guarantee.

8. Logic symbols (digital circuits)

Graphical logic symbols accord with MIL standard 806B.
Supplementary drawings correlate logic functions with pin locations as a help to laying out printed circuit boards.

9. Outline drawing and pin 1 identification

Dimensional drawings indicate the pin numbering of circuit packages.
Dual in-line packages have a notch at one end to identify pin 1.
Take care not to mistake adventitious moulding marks for the pin 1 identification.
Flat packs identify pin 1 by a small projection on the pin itself and/or by a dot on the body of the package.
Metal can encapsulations identify pin 1 by a tab on the rim of the can.

PRO ELECTRON TYPE DESIGNATION CODE

The type number consists of three letters followed by a four digit serial number (sometimes augmented by a version letter).

First two letters:

Family circuits

The first two letters identify the family.

Solitary circuits

The first letter identifies the circuit as:

S-digital
T-analogue
U-mixed analogue/digital

The second letter has no special significance.

The third letter indicates the operating ambient temperature range or another significant characteristic. Letters B to F stand for the following temperature ranges: [1])

B: 0 to +70 °C
C: -55 to +125 °C
D: -25 to +70 °C
E: -25 to +85 °C
F: -40 to +85 °C

When no temperature range is specified, the third letter is A. Other third letters identify special family versions or treatments (e.g. radiation hardened).

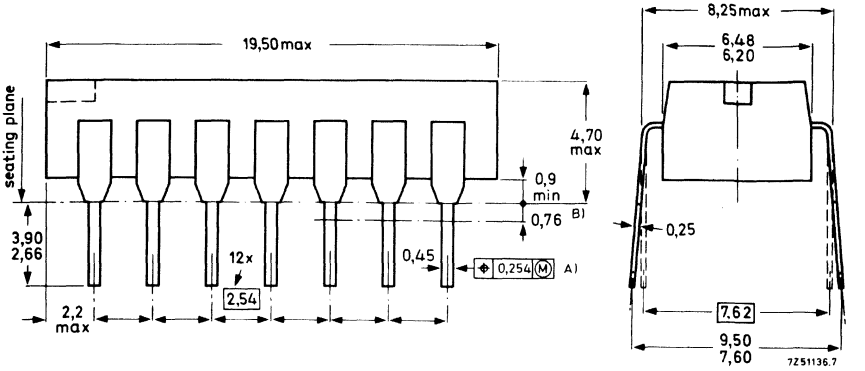
The serial number following the three letters may be either a 4-digit number or a proprietary type designation comprising a combination of letters and digits. Proprietary type designations consisting of less than 4 characters are extended to 4 by putting zeros (0) before them.

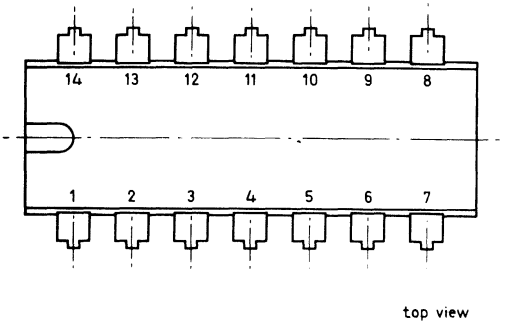
[1]) If a circuit is published for a wider temperature range, but does not qualify for another classification, the letter designating the nearest narrower temperature range is used.

Package outlines

14 LEAD PLASTIC DUAL IN-LINE (type A)

Dimensions in mm





A) Centre-lines of all leads are within ± 0,127 mm of the nominal positons shown; in the worst case, the spacing between any two leads may, deviate from nominal by ±0,254 mm.

B) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

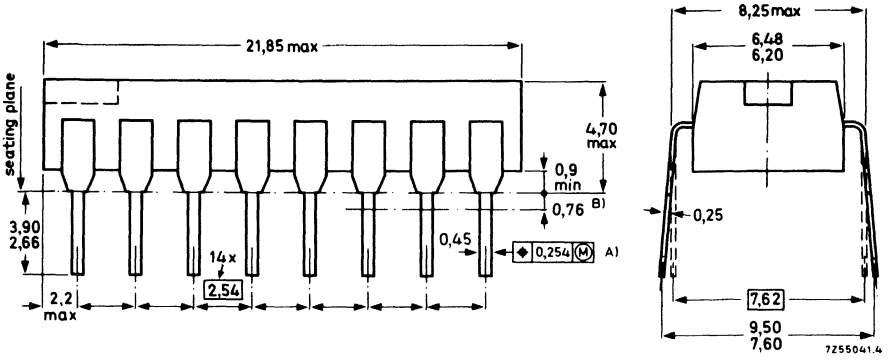
   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

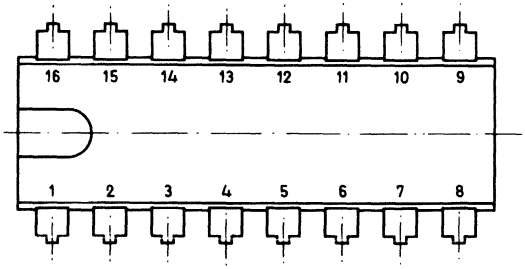
3. Repairing soldered joints

   The same precautions and limits apply as in (1) above.

16 LEAD PLASTIC DUAL IN-LINE (type A)

Dimensions in mm





top view

A) Centre-lines of all leads are within ±0,127 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B) Lead spacing tolerances apply from seating plane to the line indicated

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

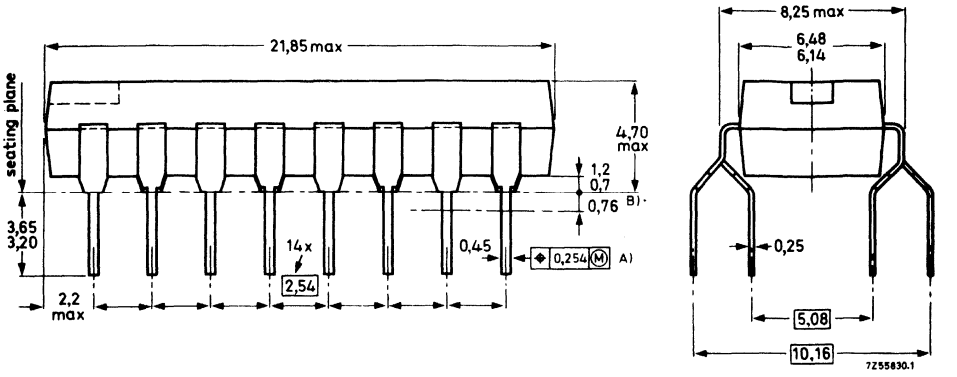
   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

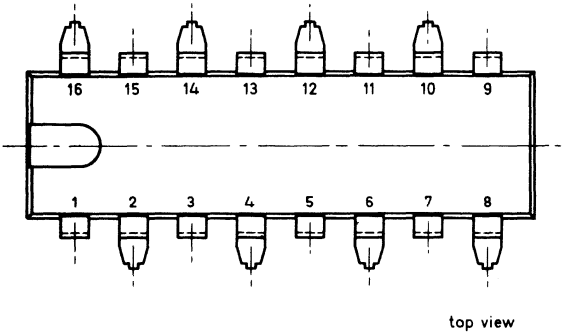
3. Repairing soldered joints

   The same precautions and limits apply as in (1) above.

16 LEAD PLASTIC QUADRUPLE IN-LINE

Dimensions in mm





A) Centre-lines of all leads are within ±0,127 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

   The same precautions and limits apply as in (1) above.

RATING SYSTEMS

ACCORDING TO I.E.C. PUBLICATION 134

1. DEFINITIONS OF TERMS USED

1.1 Electronic device. An electronic tube or valve, transistor or other semiconductor device.
Note: This definition excludes inductors, capacitors, resistors and similar components.

1.2 Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

1.3 Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

1.4 Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.
Note: Limiting conditions may be either maxima or minima.

1.5 Rating system. The set of principles upon which ratings are established and which determine their interpretation.
Note: The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

2. ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

p.t.o.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

3. DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

4. DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

NOTE

It is common use to apply the Absolute Maximum System in semiconductor published data.

LETTER SYMBOLS FOR LINEAR INTEGRATED CIRCUITS

General

The voltages and currents are normally related to the terminals to which they are applied or at which they appear. Each terminal is indicated by a number. In appropriate cases voltages, currents etc. pertinent to one or more of the circuit elements (transistors, diodes) are given in which case symbols are based on the recommendations as published in I.E.C. Publication 148.

Quantity symbols

1. Instantaneous values of current, voltage and power, which vary with time are represented by the appropriate lower case letter.

   Examples: i, v, p

2. Maximum (peak), average, d.c. and root-mean-square values are represented by the appropriate upper case letter.

   Examples: I, V, P

Polarity of current and voltage

A current is defined to be positive when its conventional direction of flow is into the device.
A voltage is measured with respect to the reference terminal, which is indicated by the subscripts. Its polarity is defined to be positive when the potential is higher than that of the reference terminal.

Subscripts

For currents the number behind the quantity symbol indicates the terminal carrying the current.

Examples: I_2, i_{14}

For voltages normally two number subscripts are used, connected by a hyphen. The first number indicates the terminal at which the voltage is measured and the second subscript the reference terminal.
Where there is no possibility of confusion the second subscript may be omitted.

Examples: V_{2-12}, v_{14-2}, V_5, v_8

To distinguish between maximum (peak), average, d.c. and root-mean-square values the following subscripts are added:

For maximum (peak) values : M or m
For average values : AV or av
For root-mean-square values: (RMS) or (rms)
For d.c. values : no additional subscripts

The upper case subscripts indicate total values.
The lower case subscripts indicate values of varying components:

Examples: I_2, I_{2AV}, $I_{2(rms)}$, $I_{2(RMS)}$

If in appropriate cases quantity symbols are pertinent to single elements of a circuit (transistors or diodes), the normal subscripts for semiconductor devices can be used.

Examples: V_{CBO}, V_{be}, V_{CES}, I_C

V_{DSS}, V_{GS}, I_D

List of subscripts:

E, e	=	Emitter terminal
B, b	=	Base terminal for bipolar transistors, Substrate for MOS devices
C, c	=	Collector terminal
D, d	=	Drain terminal
G, g	=	Gate terminal
S, s	=	Source terminal for MOS devices Substrate for bipolar transistor circuits
(BR)	=	Break-down
M, m	=	Maximum (peak) value
AV, av	=	Average value
(RMS), (rms)	=	R.M.S. value

Electrical Parameter Symbols

1. The values of four pole matrix parameters or other resistances, impedances, admittances, etc., inherent in the device, are represented by the lower case symbol with appropriate subscript.

Examples: h_i, z_f, y_o, k_r

Subscripts for Parameter Symbols

1. The static values of parameters are indicated by upper case subscripts.

Examples: h_{FE}, h_I

2. The small signal values of parameters are indicated by lower case subscripts.

Examples: h_i, z_o

3. The first subscript, in matrix notation identifies the element of the four pole matrix.

   i (for 11) = input
   o (for 22) = output
   f (for 21) = forward transfer
   r (for 12) = reverse transfer

   Examples: $V_1 = h_i I_1 + h_r V_2$

   $I_2 = h_f I_1 + h_o V_2$

The voltage and current symbols in matrix notation are indicated by a single digit subscript.
The subscript 1 = input; the subscript 2 = output.
The voltages and currents in these equations may be complex quantities.

4. A second subscript is used only for separate circuit elements (e.g. transistors) to identify the circuit configuration:

   e = common emitter
   b = common base
   c = common collector

5. If it is necessary to distinguish between real and imaginary parts of the four pole parameters, the following notation may be used:

   R_e (h_i) etc. ... for the real part
   I_{m} (h_i) etc. ... for the imaginary part

LIST OF LETTER SYMBOLS IN ALPHABETICAL ORDER

Letter symbol	Definition
B	Bandwidth
b_i, b_o	Input, respectively output susceptance
C_i, C_o	Input, respectively output capacitance
CMMR	Common-mode rejection ratio
d	Distortion
F	Noise figure
f	Frequency
f_c	Cut-off frequency
f_o	Centre frequency, intermediate frequency
fm	Modulation frequency
f_T	Transition frequency
g_i, g_o	Input, respectively output conductance
G_p	Power gain
G_{tr}	Transducer gain
G_v	Voltage gain
h_F, h_{FB}, h_{FC}, h_{FE}	DC current gain (output voltage held constant)
h_f, h_{fb}, h_{fc}, h_{fe}	Small signal current gain (output short-circuited to a.c.)
I_3, I_B, I_C, I_E, I_D, I_Q, I_S	Total d.c. current
i_3, i_B, i_C, i_E, i_D, i_G, i_S	Instantaneous total value of the current
I_{3AV}, I_{BAV}, I_{CAV}, I_{EAV}	Total average current
I_{3M}, I_{BM}, I_{CM}, I_{EM}	Maximum (peak) value of the total current
I_{3m}, I_{bm}, I_{cm}, I_{em}	Maximum (peak) value of the varying component of the current
I_{CBO}	Collector cut-off current (open emitter)
I_{CS}	Collector-substrate leakage current
I_{DSS}	Drain cut-off current (source short-circuited to gate)

Letter symbol	Definition
I_{EBO}	Emitter cut-off current
I_I, I_i	Input current of a specified circuit
I_{io}	Input offset current
I_O, I_o	Output current of a specified circuit
I_{OM}	Peak value of output current
$I_{o(p-p)}$	Peak to peak value of output current
I_{tot}	Total supply current
K_f	Small signal voltage gain
K_o	Output impedance (see K parameters)
K_r	Reverse current transfer ratio
M	Modulation depth
P_i, P_o	Input, respectively output power of a specified circuit
P_{tot}	Total power dissipation in the device
R_i, R_o	Input, respectively output resistance of a specified circuit
R_L	Load resistance
R_S	Source resistance
R_{th}	Thermal resistance
SVRR	Supply voltage rejection ratio
T_{amb}	Ambient temperature
T_{case}	Case temperature
T_{stg}	Storage temperature
V_3, V_{3-4}, V_{BE}, V_{CB}	Total value of the voltage (d.c.)
v_3, v_{3-4}, v_{BE}, v_{CB}	Instantaneous value of the total voltage
V_{BEsat}, V_{CEsat}	Saturation voltage at specified bottoming conditions
$V_{(BR)CBO}$, $V_{(BR)CEO}$, $V_{(BR)EBO}$	Breakdown voltage between the terminal of the first subscript and the reference terminal (second subscript) when the third terminal is open circuited
$V_{(BR)CS}$	Collector to substrate breakdown voltage
V_{CBO}, V_{CEO}, V_{EBO}, V_{CS}, V_{1-3}	Voltage of the terminal indicated with respect to the reference terminal (second subscript)

Letter symbol	Definition
V_i, V_o	Input, respectively output voltage of a specified circuit
V_{io}	Input offset voltage
$V_{i\ lim}$	Input voltage at which limiting starts
V_N	Negative supply voltage
V_P	Positive supply voltage
V_n	Noise voltage
y_i, y_f, y_o, y_r	Input, transfer, output and feedback admittance
Z_i, Z_o	Input, respectively output impedance
η	Efficiency
φ_i, φ_f, φ_o, φ_r	Phase angle of input, transfer, output and feedback admittance

Linear integrated circuits

Audio

Hearing aids	OM200/S2	Integrated amplifier for use in hearing aids
	TAA370	Hearing aid amplifier
Low power	TAA263	Low-level amplifier
	TAA310; A	A.F. preamplifier
	TAA320	Integrated MOST amplifier
	TBA915	Audio amplifier
	TCA210	Audio amplifier and preamplifier
	TCA490A to C	Dual operational amplifier and stereo preamplifier
Power output	TCA160; B	Integrated power audio amplifier

Radio

A.M./F.M. receiver circuits	TBA570	Integrated a.m./f.m. radio receiver circui
	TBA690	Integrated a.m./f.m. radio receiver circui
	TBA700	Integrated a.m./f.m. radio receiver circui
Stereo decoder	TCA290A	F.M. stereo decoder
I.F. amplifier	TCA420A	I.F. amplifier

Television

R.F. and I.F.	TBA480	I.F. amplifier
	TBA750A	Limiter amplifier
	TCA270	Television signal processing circuit
	TCA540	Synchronous demodulator for tv receivers
Signal processing	TBA550	Television signal processing circuit
	TBA720	Line oscillator circuit (tubes)
	TBA720A	Line oscillator circuit (transistors)
	TBA890	Television signal processing circuit
	TBA900	Television signal processing circuit
	TBA920	Horizontal combination
Colour decoding	TAA630S; T	Synchronous demodulator for colour difference drive
	TBA500N; P	Luminance combination
	TBA510	Chrominance combination
	TBA520	Colour demodulator
	TBA530	R.G.B. matrix preamplifier
	TBA540	Reference combination
	TBA560B	Luminance and chrominance control combination
	TBA560C	Luminance and chrominance control combination
	TBA990	Colour demodulator
Voltage stabilizer	TAA550	Voltage stabilizer

General industrial

Operational amplifiers	TBA221; B; D	Operational amplifier
	TBA222	Operational amplifier
	TCA220	Triple operational amplifier
	TCA410A; B	Voltage follower
	TCA490A to C	Dual operational amplifier and stereo preamplifier
	TCA520B	Operational amplifier
Voltage regulators	TBA281	Voltage regulator

Telecommunication

Microphone amplifiers	TAA970	Microphone amplifier
	TBA880	Microphone amplifier
Modulators/demodulators	TAB101	Ring (de)modulator for telephony and industrial equipment
	TBA673	
Audio amplifiers	TAA480	Low frequency amplifier
	TAA960	Triple amplifier for active filters
	TBA915	Audio amplifier
	TCA210	Audio amplifier and preamplifier

Miscellaneous

SAJ110	Bi-polar frequency divider
SAJ250A; B	32 kHz clock circuit
TAA263	Low-level amplifier
TAA320A	Integrated MOST level sensor
TBA281	Voltage regulator

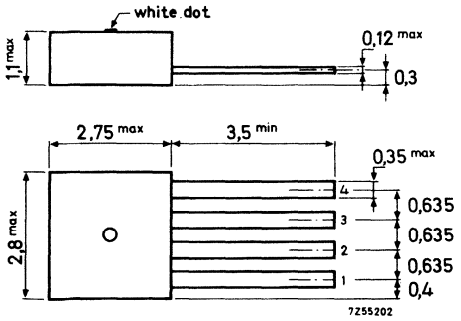
INTEGRATED AMPLIFIER

for use in ear hearing aids

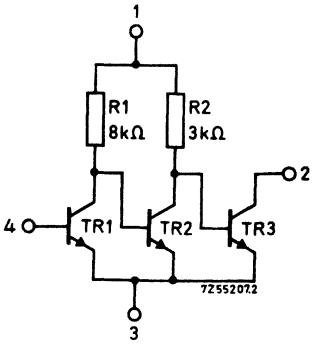
Monolithic integrated circuit amplifier in a plastic envelope, primarily intended for use in ear hearing aids.

QUICK REFERENCE DATA				
For meaning of symbols see test circuit on page 3				
Supply voltage	V_{1-3}	max.	5	V
Supply current	I_2	max.	5	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	25	mW
The following data are measured in test circuit on page 3				
Total supply current	I_{tot}	typ.	1	mA
Transducer gain	G_{tr}	>	77	dB
		typ.	85	dB
Output power at d_{tot} = 10%	P_o	>	0,2	mW
Cut-off frequency (−3 dB)	f_c	>	20	kHz

PACKAGE OUTLINE (Dimensions in mm)



CIRCUIT DIAGRAM



The sealing of the plastic envelope withstands the accelerated damp heat test of IEC recommendation 68-2 (test D, severity IV, 6 cycles).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

For meaning of symbols test circuit on page 3.

Voltages

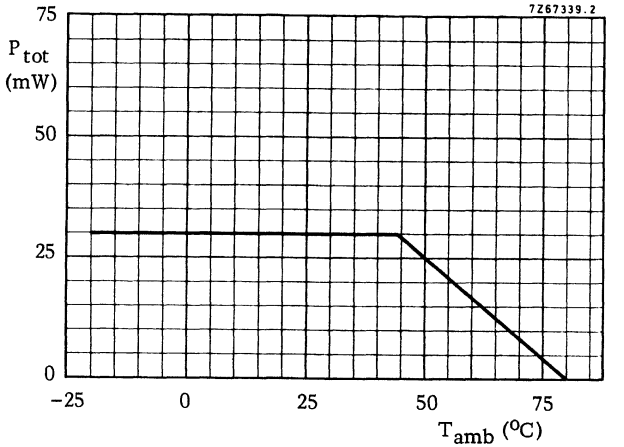
Supply voltage	V_{1-3}	max.	5	V
Output voltage	V_{2-3}	max.	5	V [1]
Input voltage	$-V_{4-3}$	max.	5	V

Currents

Output current	I_2	max.	5	mA
Input current	I_4	max.	5	mA

Power dissipation

Power derating curve



Temperatures

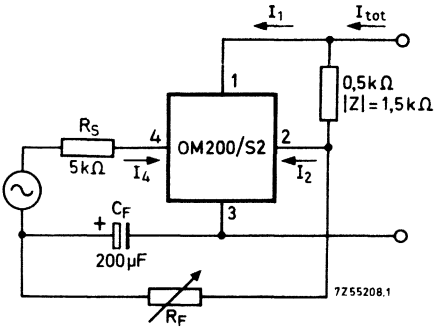
Storage temperature	T_{stg}	−20 to +80	°C
Ambient temperature (see derating curve above)	T_{amb}	−20 to +80	°C

1) This value may be exceeded during inductive switch-off for transient energies < 10 μWs.

CHARACTERISTICS at $V_{1-3} = 1,3\ V$; $I_2 = 0,7\ mA$ and $T_{amb} = 25\ ^oC$ unless otherwise specified

Supply currents (no signal)	I_{tot}	<	1,1	mA	
	I_1	typ.	0,30	mA	
Transducer gain at f = 1 kHz	G_{tr}	>	77	dB	1)
		typ.	85	dB	
Total distortion at f = 1 kHz					
P_o = 100 µW	d_{tot}	typ.	4	%	
		<	6	%	
P_o = 200 µW	d_{tot}	<	10	%	
Noise figure at R_S = 5 kΩ					
B = 400 to 3200 Hz	F	typ.	2,5	dB	
		<	6	dB	2)
Cut-off frequency (−3 dB)	f_c	>	20	kHz	
Value of R_F to adjust I_2 at 0,7 mA	R_F		170 to 1000	kΩ	
		typ.	400	kΩ	

Test circuit



Note

$I_2 = 0,7\ mA$; adjusted by means of R_F
$V_{1-3} = 1,3\ V$; $T_{amb} = 25\ ^oC$

1) The transducer gain is defined as the ratio of the output power in the load $|Z| = 1,5\ k\Omega$ and the available input power of the source with $R_S = 5\ k\Omega$.

$$G_{tr} = \frac{P_o}{V_i^2/4\,R_S}$$

2) Due to special processing and pre-measuring, the flutter-noise level is extremely low.

SOLDERING RECOMMENDATIONS

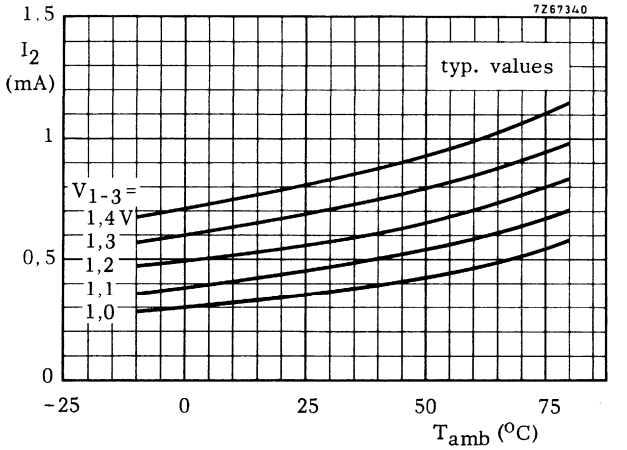
1. Iron soldering

   At a maximum iron temperature of 300 °C the maximum permissible soldering time is 3 seconds, provided the solder spot is at least 0,5 mm from the seal and the leads are not soldered at the same time. Soldering in immediate subsequence is allowed.

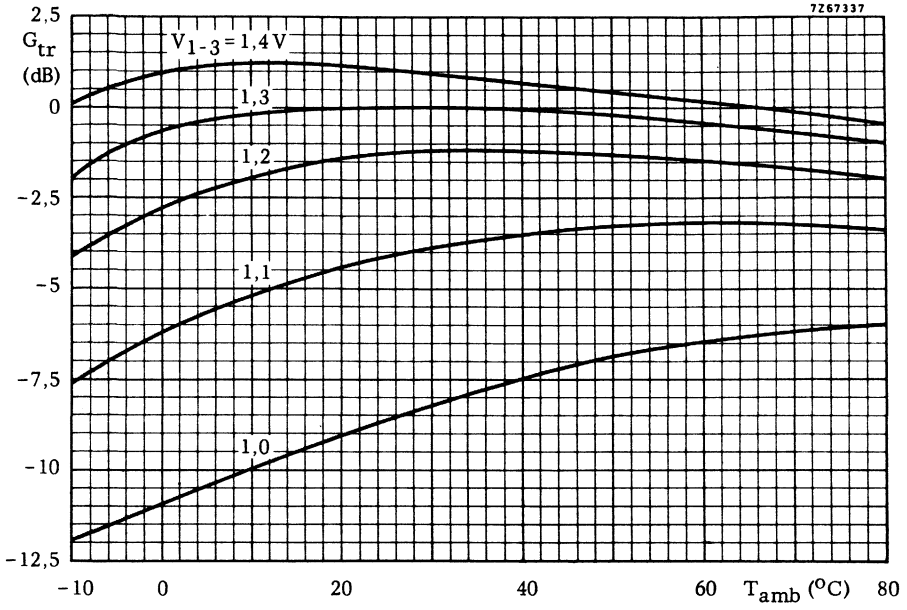
2. Dipsoldering

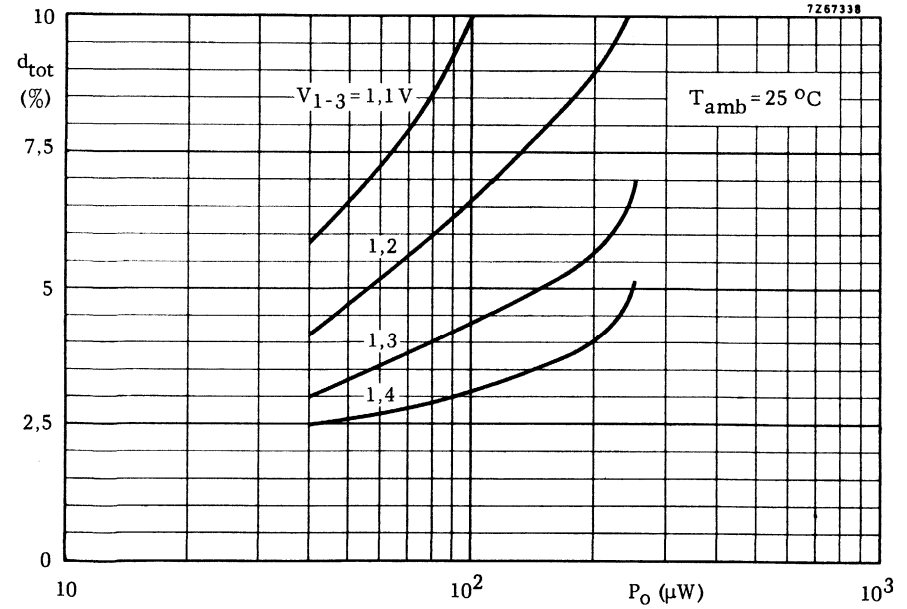
   At a maximum solder temperature of 250 °C the maximum permissible soldering time is 3 seconds, provided the soldered spot is at least 0,5 mm from the seal.

CHARACTERISTICS



The graph applies to test circuit on page 3


7Z67337
2,5
G_{tr}
(dB)
0
-2,5
-5
-7,5
-10
-12,5
V_{1-3} = 1,4 V
1,3
1,2
1,1
1,0
-10
0
20
40
60
T_{amb} (°C)
80


7Z67338
10
d_{tot}
(%)
7,5
5
2,5
0
V_{1-3} = 1,1 V
1,2
1,3
1,4
T_{amb} = 25 °C
10
10^2
P_o (μW)
10^3

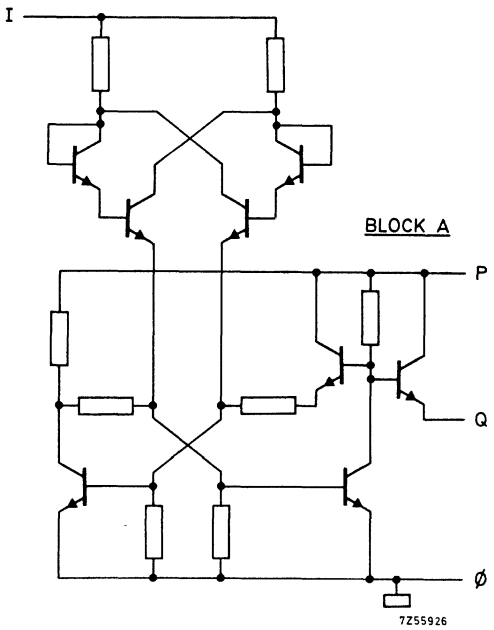
BI-POLAR FREQUENCY DIVIDER

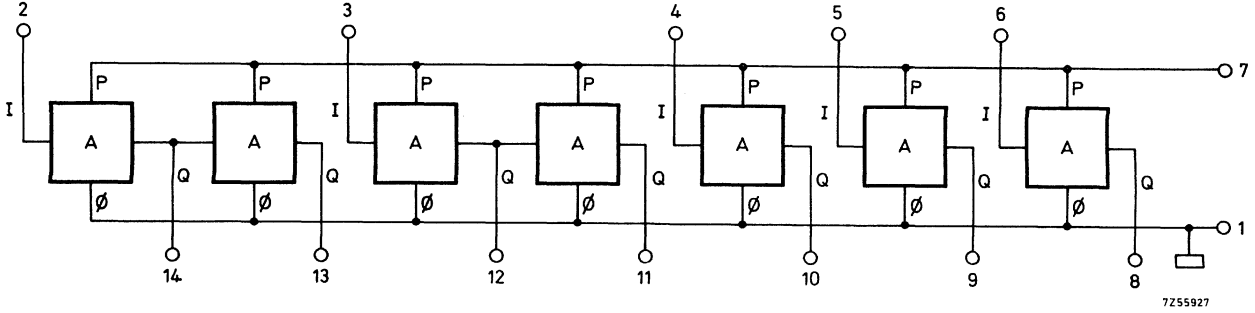
The SAJ110 is a monolithic integrated circuit in bipolar technique, consisting of 7 binary frequency dividers separated in groups of 2, 2, 1, 1 and 1, each section having its own trigger input.
The circuit consists of a d.c. flip-flop and can accept any input waveform, making the device particularly suitable for use in electronic organs. The output impedance is low and there is excellent separation between adjacent stages.

QUICK REFERENCE DATA				
Supply voltage	$V_{7-1} = V_P$	nom.	9	V
Ambient temperature	T_{amb}	nom.	25	°C
Input voltage levels	V_{IL}	≤	1	V
	V_{IH}	≥	6	V
		≤	V_{7-1}	
Output voltage levels	V_{OL}	≤	0,1	V
	V_{OH}	≥	7,3	V
Output impedance (V_O in HIGH state)	$\lvert Z_o \rvert$	typ.	120	Ω
Total power dissipation every output loaded with R_L = 2,2 kΩ	P_{tot}	typ.	200	mW

PACKAGE OUTLINE 14 lead plastic dual in-line (type A)(See General Section).

CIRCUIT DIAGRAM





RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

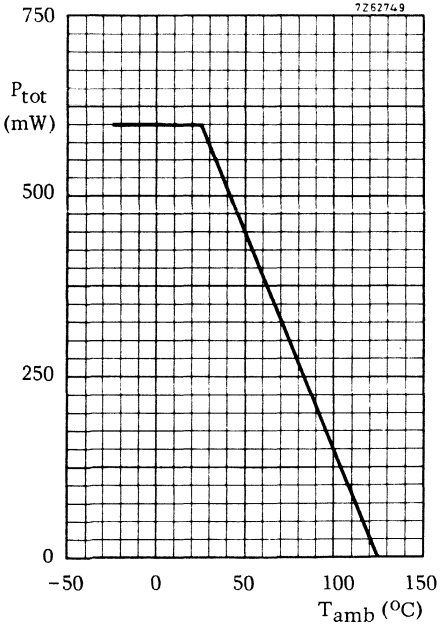
Voltages

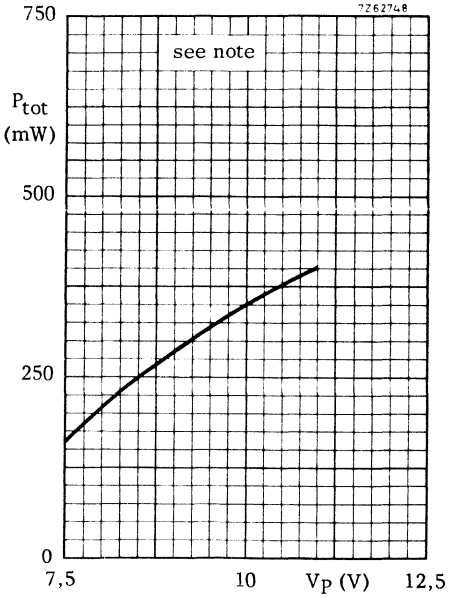
Pin No. 2; 3; 4; 5; 6 voltage with respect to pin No. 1 (substrate)	$\|V_I\|$	max. V_{7-1}	[1]
Pin No. 7 (supply voltage)	$V_{7-1} = V_P$	0 to +11	V
Pin No. 8; 9; 10; 11; 12; 13; 14 voltage	V_O	0 to +5	V
All other pins connected to pin No. 1 (substrate)			

Temperature

Storage temperature	T_{stg}	−55 to +125	°C
Operating ambient temperature (see derating curve below)	T_{amb}	−25 to +125	°C

Total power dissipation





Note Power dissipation when all flip-flop outputs are operating at maximum dissipation (extreme condition). In organ practice the average power dissipation is less because the master oscillators cause the flip-flops to switch continuously.

[1]) Negative going input signals cause some distortion in the output pulse so that an optimal application using only positive going input signals as advised.

CHARACTERISTICS

Supply voltage	$V_{7-1} = V_P$		7,5 to 11	V	
		typ.	9	V	

CHARACTERISTICS at V_P = 9 V; T_{amb} = 25 °C; R_L = 2,2 kΩ (see Fig. 1 on page 5).

Input voltage levels	V_{IL}	≤	1	V	1)
	V_{IH}		6 to V_P	V	1)
Output voltage levels	V_{OL}	≤	0,1	V	2)
	V_{OH}	≥	7,3	V	2)
Change-over time	t_c	≤	0,2	µs	3)
Dynamic input impedance	$\|Z_i\|$	typ.	8	kΩ	4)
Output impedance (V_O in HIGH state)	$\|Z_o\|$	typ.	120	Ω	
Total power dissipation	P_{tot}	typ.	200	mW	5)
Supply current per divider	I_7	≤	3	mA	6)
Output current (per stage)	I_o	≤	5	mA	7)
Frequency range (input)	f_I		20 Hz to 20	kHz	8)
Resetting of divider at :	I_o	typ.	50	mA	9)

1) See also Fig. 2 on page 5 and Fig. 4 on page 6.

2) See also Fig. 3 on page 5, Fig. 5 and Fig. 6 on page 6.

3) See also Fig. 3 on page 5.

4) See also Fig. 7 on page 6.

5) Typical value under condition that all flip-flop outputs are operating at max. dissipation.

6) Measured when output stage is in LOW state.

7) Occasional short circuiting pins 8, 9, 10, 11, 12, 13 and 14 is allowed; the output currents are internally limited to about 100 mA.

8) This range is based on requirements for applications in organs; in practice the frequency range is much larger (from d.c. to about 1 MHz).

9) Input voltage must be in LOW state.

CHARACTERISTICS (continued)

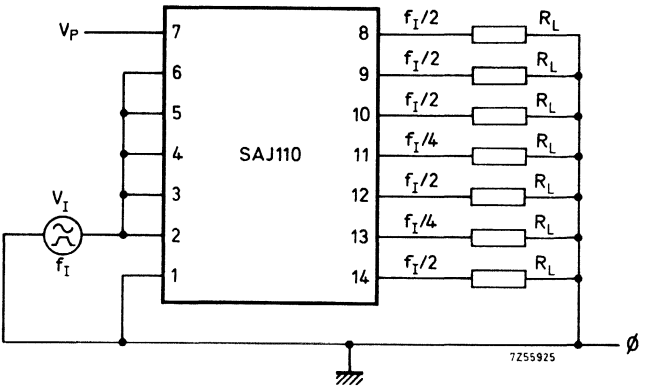


Fig. 1 Test circuit

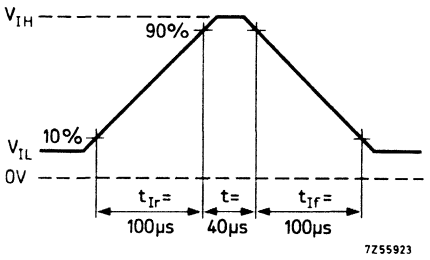


Fig. 2 Input voltage: V_I

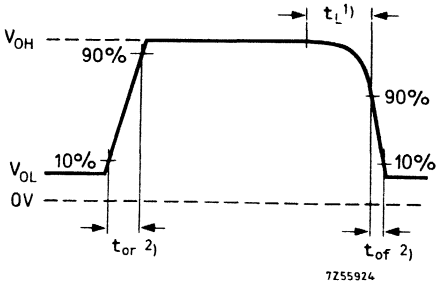


Fig. 3 Output voltage: V_O

1) t_L is depending on the slope of the input signal

2) change-over time: $t_c = \frac{t_{or} + t_{of}}{2}$

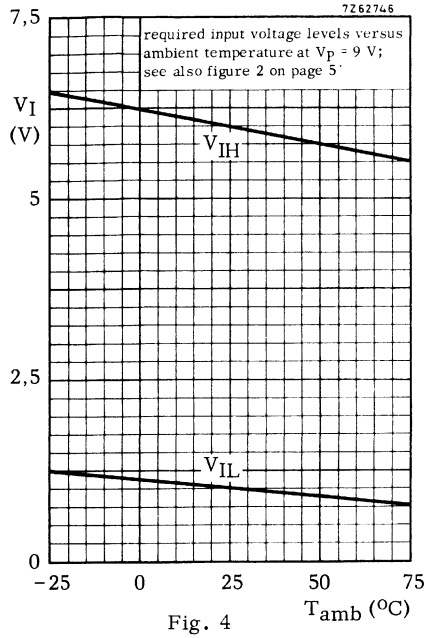


Fig. 4

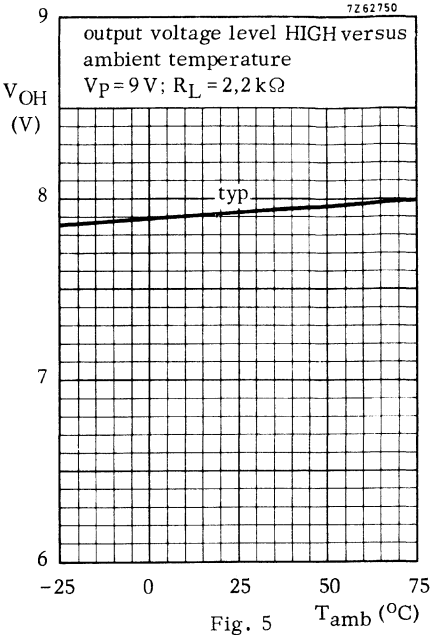


Fig. 5

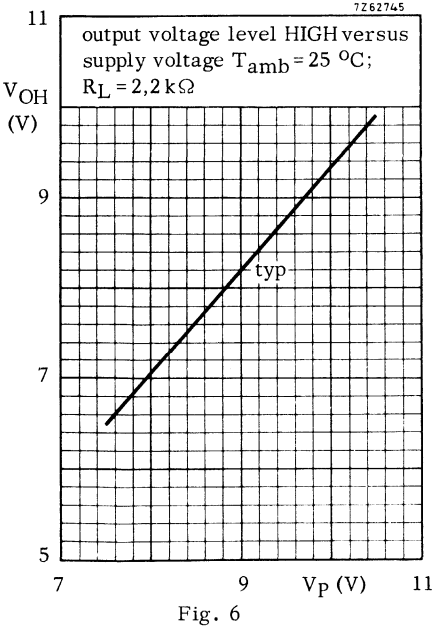


Fig. 6

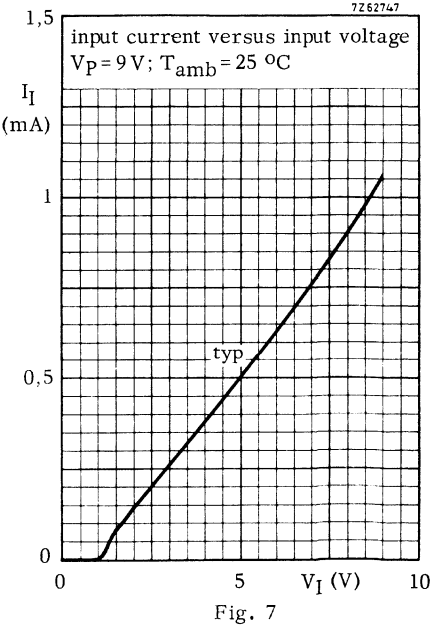


Fig. 7

32 kHz CLOCK CIRCUIT

The SAJ250 is a monolithic integrated circuit which contains the complete electronics needed for a battery operated 32 kHz quartz crystal controlled clock. It consists of an oscillator, a 15-stage frequency divider, a driver for a stepping motor and a supply current regulator.

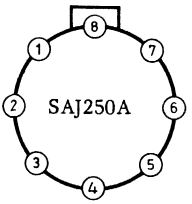
For an oscillator frequency of 32 768 Hz, the output is a 1 Hz pulse with a duration of 31,25 ms and a current drive capability of 15 mA. A built-in regulation circuit allows to regulate the voltage across the load at 1,2 V for a supply voltage between 1,3 and 1,8 V.

The circuit works with a supply voltage between 0,9 V and 3 V; at 1,3 V, the current requirement is 24 μA.

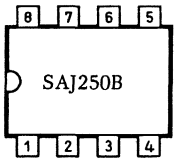
QUICK REFERENCE DATA				
Frequency division			$2^{15} = 32768$	
Supply voltage range	V_P		0,9 to 3	V
Supply current	I_P	typ.	24	μA
Output current	I_O		15	mA

PACKAGE OUTLINES See page 2

CONNECTION DIAGRAM AND PINNING



1. quartz crystal connection
2. output regulation
3. output
4. ground
5. positive supply (V_P)
6. not connected
7. not connected
8. quartz crystal connection

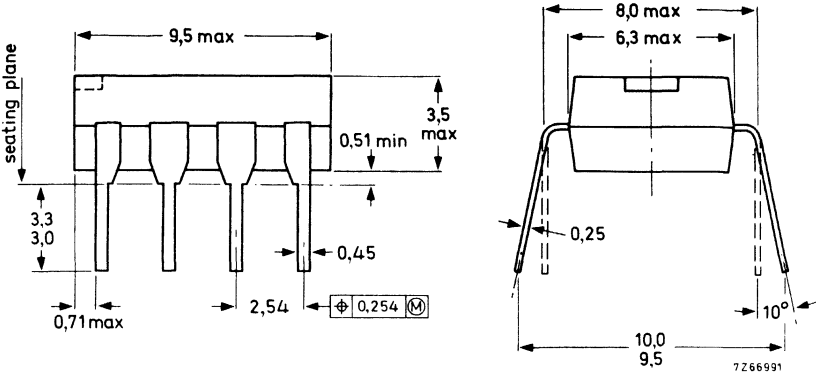


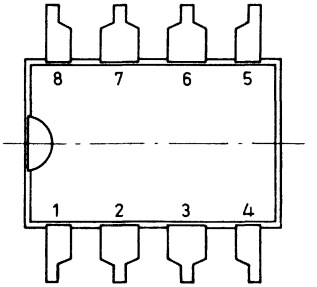
1. output regulation
2. output
3. ground
4. positive supply (V_P)
5. not connected
6. not connected
7. quartz crystal connection
8. quartz crystal connection

PACKAGE OUTLINES

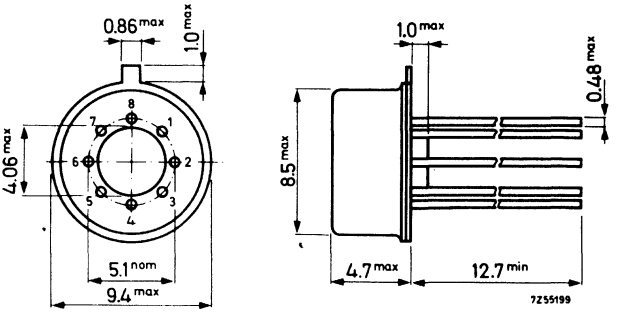
Dimensions in mm

8 lead plastic dual in-line : SAJ250B

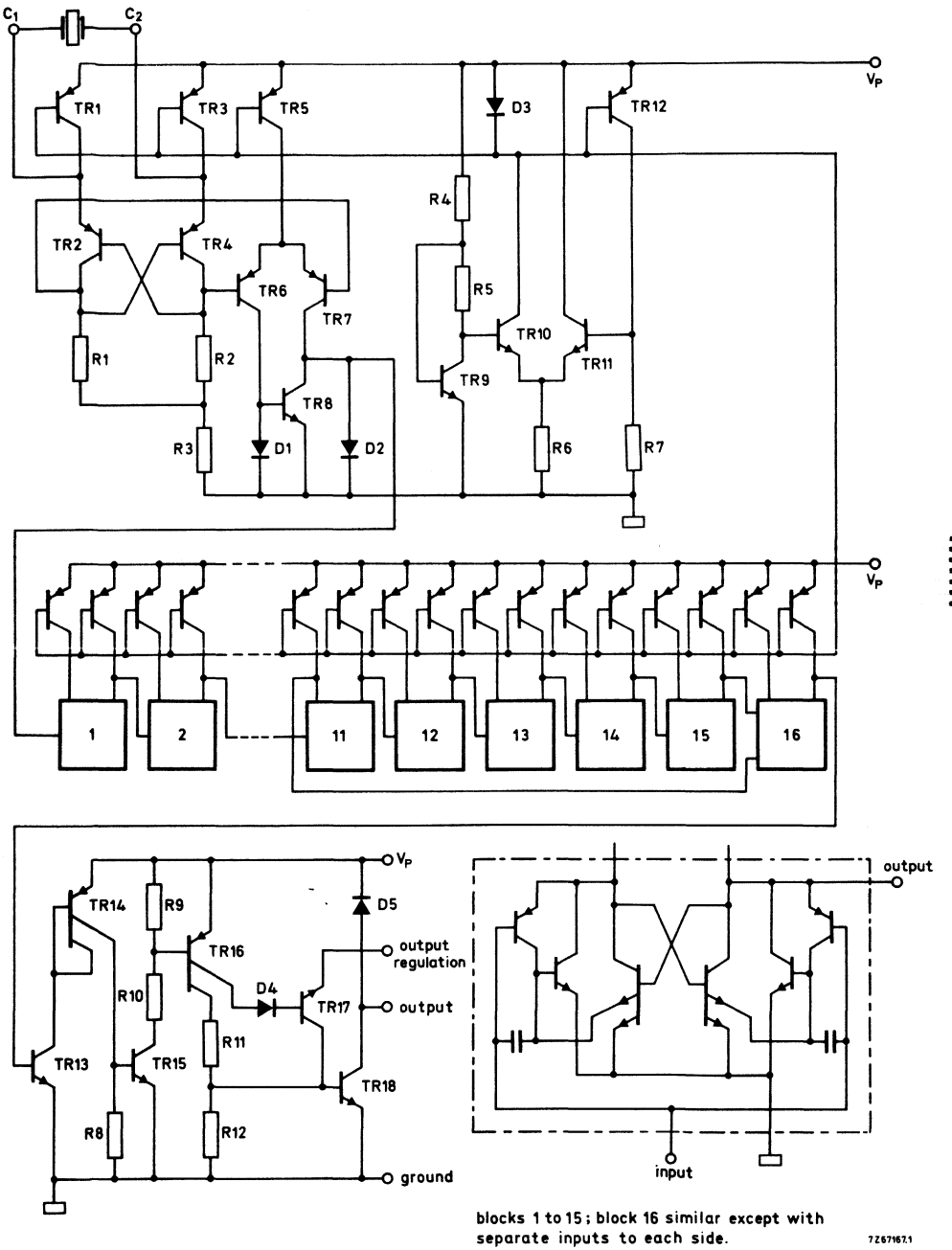




TO-99 metal envelope : SAJ250A



CIRCUIT DIAGRAM



blocks 1 to 15; block 16 similar except with separate inputs to each side.

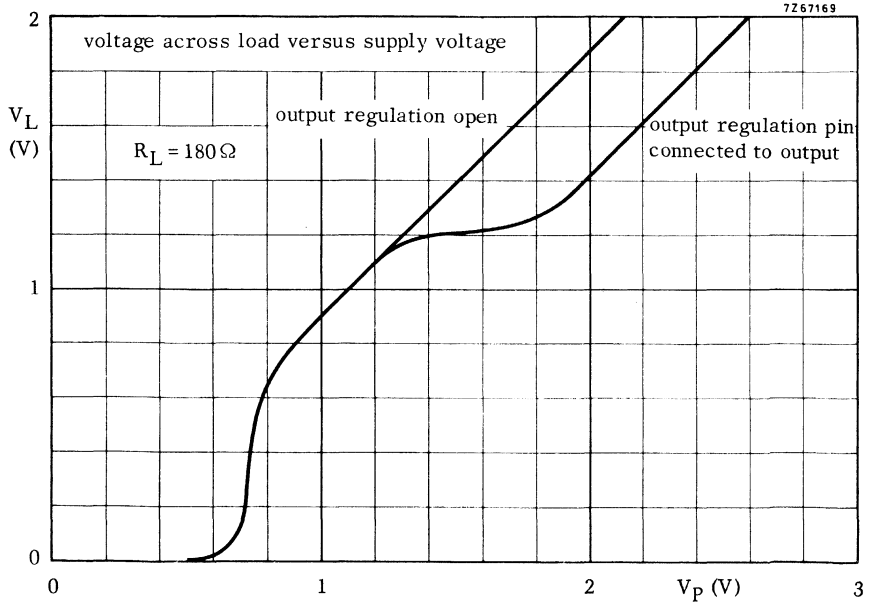
7Z67167.1

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Supply voltage	V_P	max.	3 V
Output current	$\pm I_o$	max.	50 mA
Operating temperature	T_{amb}		-10 to +60 °C
Storage temperature	T_{stg}		-55 to +100 °C

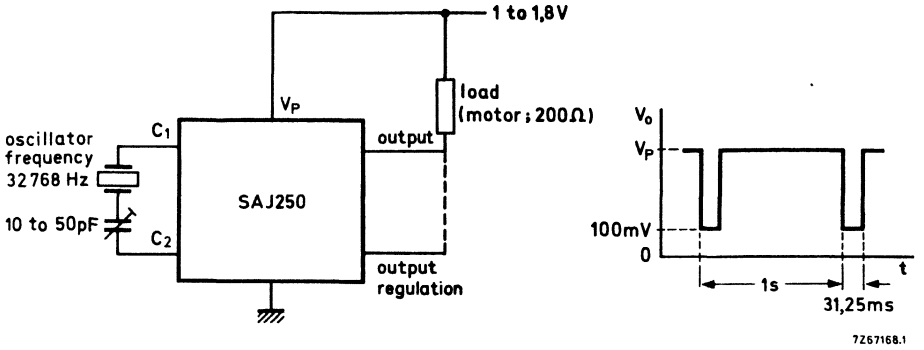
CHARACTERISTICS at V_P = 1,3 V; f_{osc} = 32 768 Hz; T_{amb} = 25 °C unless otherwise specified

Supply voltage range	V_P		0,9 to 3 V
Supply current (output open)	I_P	typ. <	24 µA 32 µA
Output frequency	f_o	nom.	1 Hz
Output pulse duration	t_p	nom.	31,25 ms
Output pulse current at V_o = 200 mV	I_o	typ.	15 mA
Regulated output voltage across load (output regulation pin connected to output)	V_L	typ.	1,2 V
Negative oscillator resistance	R_{osc}	> typ.	50 kΩ 80 kΩ
Stability of oscillator for ΔV_P = 100 mV	$\frac{\Delta f}{f_{osc}}$	typ.	$2 \cdot 10^{-7}$



APPLICATION INFORMATION

32 kHz quartz crystal controlled clock



The output regulation pin is left open for an unregulated output voltage. With the output regulation pin connected to the output pin, the output voltage across the load is regulated at 1, 2 V for a supply voltage between 1, 3 V and 1, 8 V.

A built-in clamping diode between the output and the positive supply terminal acts as current by-pass if the induced voltage of the stepping motor exceeds 0, 6 V.
A trimming capacitor is used in series with the quartz crystal to adjust for correct operating frequency.

LOW-LEVEL AMPLIFIER

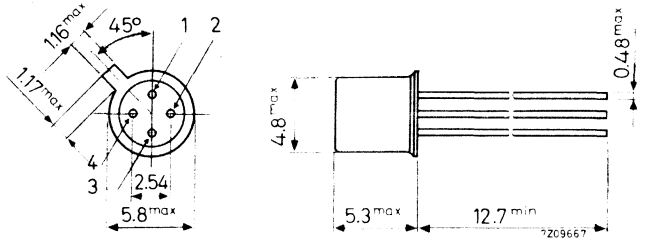
The TAA263 is a semiconductor integrated amplifier in a 4-lead TO-72 metal envelope. It comprises a three-stage, direct coupled low-level amplifier for use from d.c. up to frequencies of 600 kHz.

QUICK REFERENCE DATA				
Supply voltage	V_B	max.	8	V
Output voltage	V_{3-4}	max.	7	V
Output current	I_3	max.	25	mA
Transducer gain at P_o = 10 mW				
R_L = 150 Ω; f = 1 kHz	G_{tr}	typ.	77	dB
Operating ambient temperature	T_{amb}	−20 to +100		°C

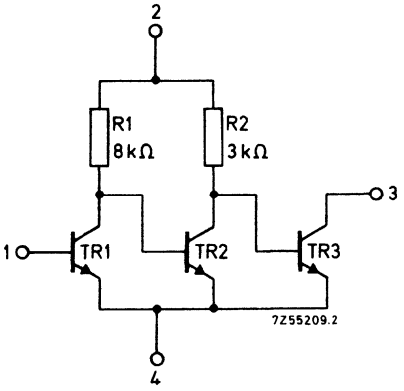
PACKAGE OUTLINE

Dimensions in mm

TO-72



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

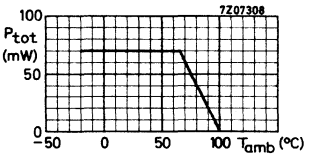
Supply voltage	V_B	max.	8	V
Output voltage	V_{3-4}	max.	7	V
Input voltage	$-V_{1-4}$	max.	5	V

Currents

Output current	I_3	max.	25	mA
Input current	I_1	max.	10	mA

Power dissipation

Total power dissipation up to $T_{amb} = 65\ ^oC$	P_{tot}	max.	70	mW



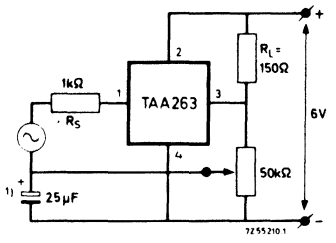
Temperatures

Storage temperature	T_{stg}	−55 to +125	°C
Operating ambient temperature (see derating curve above)	T_{amb}	−20 to +100	°C

CHARACTERISTICS

T_{amb} = 25 °C

Test circuit:



Currents				
Output current	I_3	typ.	12	mA
Total current drain (no signal)	I_2+I_3	<	16	mA
Over-all small signal current gain				
f = 1 kHz	$h_{f\ tot}$	typ.	5.10^5	
Transducer gain				
f = 1 kHz; P_o = 10 mW	G_{tr}	>	70	dB
		typ.	77	dB
Output power at f = 1 kHz; d_{tot} = 10%	P_o	>	10	mW
d_{tot} = 5%	P_o	>	8	mW
Noise figure				
f = 400 Hz to 6 kHz	F	typ.	5	dB
		<	10	dB
f = 450 kHz; Δf = 5 kHz	F	typ.	2.7	dB

1) $Z \leqslant 10\ \Omega$ at f = 1 kHz

CHARACTERISTICS (continued) T_{amb} = 25 °C

y parameters (point 4 common connection)

V_B = 6 V; I_3 = 3 mA; V_{3-4} = 4.2 V

f = 1 kHz

Input admittance	$y_i = g_i$	typ.	20	$\mu\Omega^{-1}$
Transfer admittance	$y_f = g_f$	typ.	11	Ω^{-1}
Output admittance	$y_o = g_o$	typ.	60	$\mu\Omega^{-1}$

f = 450 kHz

Input conductance	g_i	typ.	15	$\mu\Omega^{-1}$
Input capacitance	C_i	typ.	14	pF
Transfer admittance	$\|y_f\|$	typ.	9.4	Ω^{-1}
Phase angle of transfer admittance	φ_f	typ.	125°	
Output conductance	g_o	typ.	20	$\mu\Omega^{-1}$
Output capacitance	C_o	typ.	13	pF

A.F. PREAMPLIFIER

The TAA310 is a monolithic integrated circuit designed for use as an a.f. high-gain preamplifier, with a very low noise figure (< 4 dB) and a high voltage gain of at least 90 dB. Because this gain can be achieved at a low load impedance (1 kΩ) and the input impedance is high, the TAA310 is specially suited for the recording and playback amplifier in tape recorders.

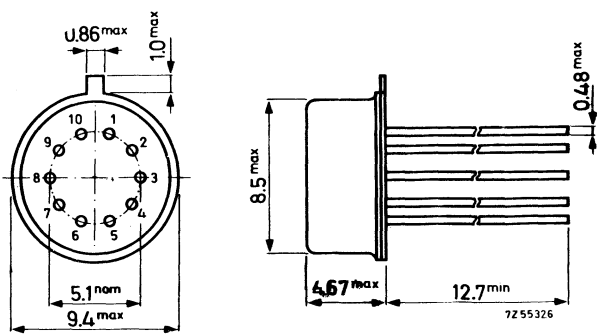
The TAA310A is the same circuit as the TAA310 except for pin connections (see page 2).

QUICK REFERENCE DATA				
Supply voltage	V_B	nom.	+7	V
Voltage gain	G_v	typ.	100	dB
Noise figure (B = 30 to 15 000 Hz)	F	typ.	2,5	dB
Input impedance	z_i	typ.	20	kΩ

PACKAGE OUTLINE

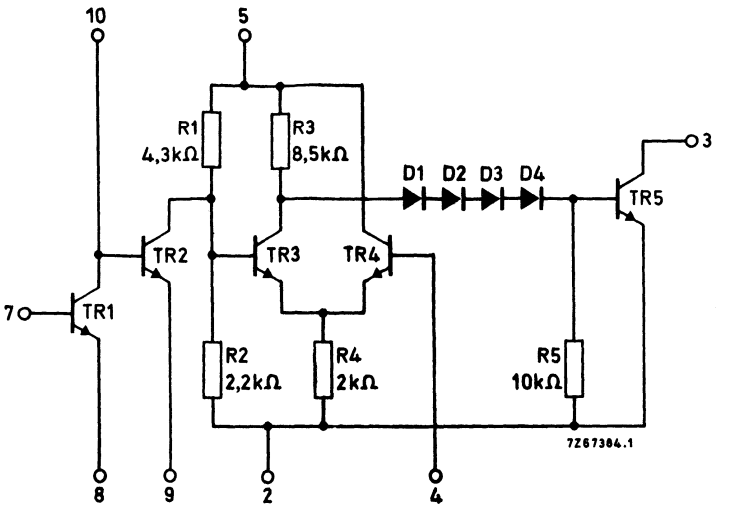
Dimensions in mm

TO-74; reduced height

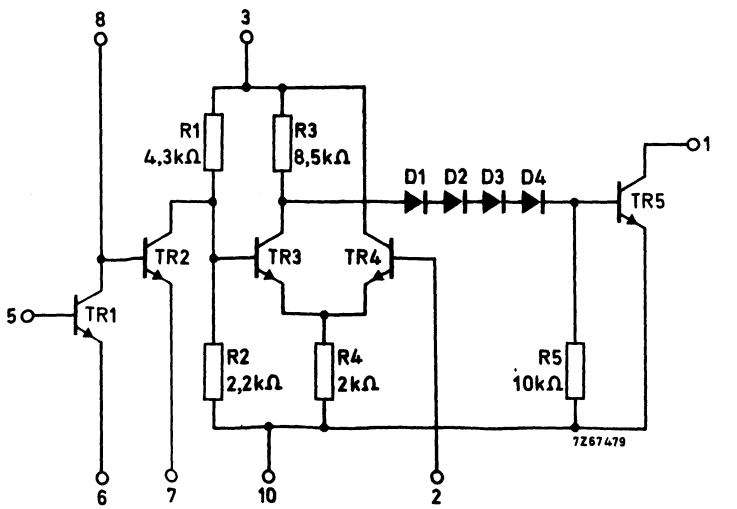


CIRCUIT DIAGRAM

TAA310



TAA310A



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

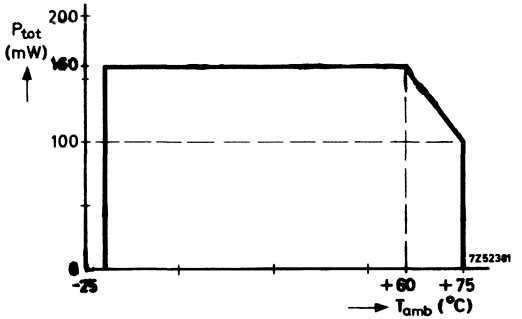
V_{5-2}	max.	9,5	V
V_{3-2}	max.	9,5	V
V_{10-8}	max.	6	V
V_{8-7}	max.	6	V
V_{9-10}	max.	6	V
V_{4-2}	max.	6	V

The pins 3, 4, 5 and 10 must never have a negative potential with respect to pin 2 (substrate).

Currents

I_3	max.	20	mA
I_7	max.	3	mA
$-I_8$	max.	10	mA
$-I_9$	max.	10	mA
I_{10}	max.	10	mA
I_4	max.	3	mA

Total power dissipation



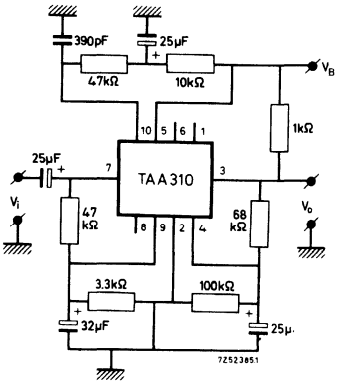
Temperatures

Storage temperature	T_{stg}	−55 to +125	°C
Operating ambient temperature (see derating curve above)	T_{amb}	−20 to +75	°C

CHARACTERISTICS at T_{amb} = 25 °C

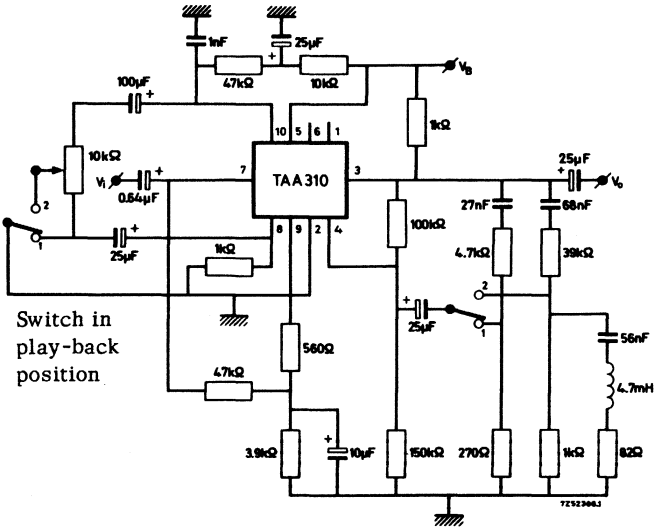
D.C. current gain				
of first transistor I_{10} = 100 μA; V_{10-7} = 0	h_{FE}	>	40	
Input impedance at f = 1 kHz				
I_{10} = 100 μA; V_{10-7} = 0	z_i	typ.	20	kΩ
Voltage gain	G_v	> typ.	93 100	dB dB
Noise figure				
R_S = 2 kΩ; B = 30 to 15 000 Hz	F	typ. <	2,5 4	dB dB
Output voltage at d_{tot} = 10%	$V_{o(rms)}$	typ.	2	V
Cut-off frequency (−3 dB)	f_c	≥	15	kHz
Saturation voltage				
of output transistor at I_3 = 7 mA	$V_{3-2\ sat}$	typ. <	0,8 1,2	V V
D.C. collector voltage				
of output transistor at I_9 = 200 μA	V_{3-2}	typ. 3,4 to 4,2	3,8	V V

Test circuit for measuring G_v, F, $V_{o(rms)}$, f_c and V_{3-2} at V_B = 7 V



APPLICATION INFORMATION

Practical tape-recorder preamplifier with a TAA310.

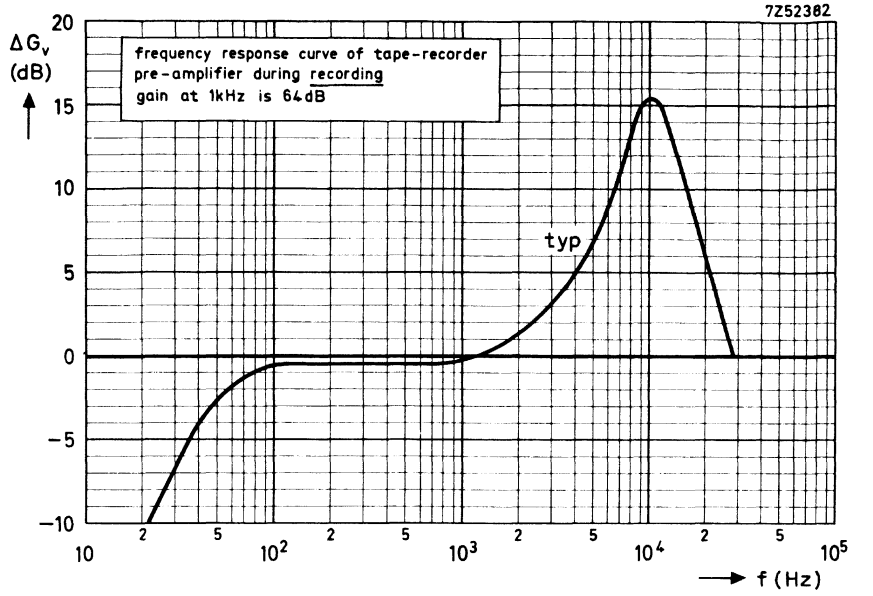


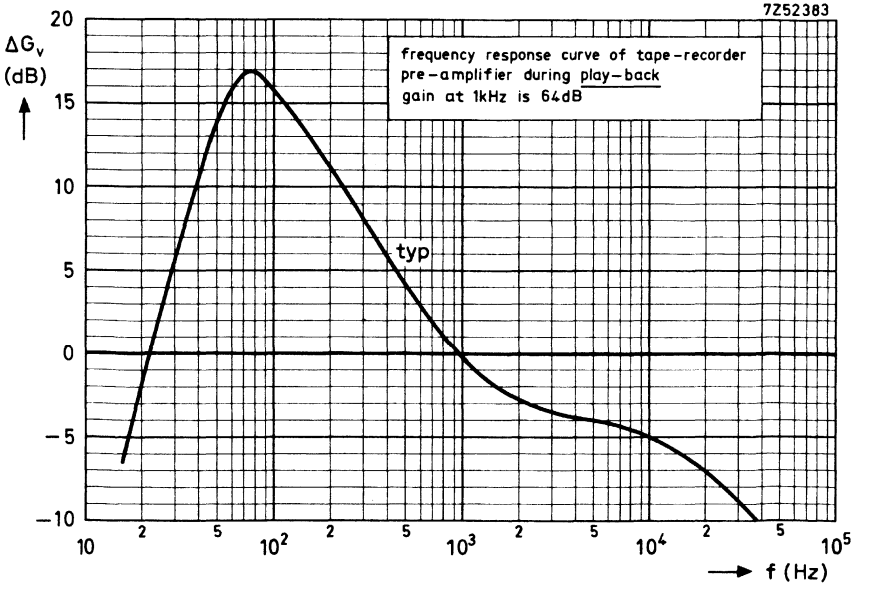
Data for use as recording amplifier (measured at f = 1 kHz)

Voltage gain	G_v		64 ± 2	dB
Frequency response (see page 6)				
Distortion at $V_{o(rms)}$ = 0.5 V	d_{tot}	<	0,5	%
Volume control range		typ.	75	dB
Signal handling		>	20	mV
Gain variation at V_B decreasing from 7 to 5 V	ΔG_v	typ.	3	dB

Data for use as play-back amplifier (measured at f= 1 kHz)

Voltage gain	G_v		64 ± 2	dB
Frequency response (see page 6)				
Distortion at $V_{o(rms)}$ = 0,5 V	d_{tot}	<	0,5	%
Gain variation at V_B decreasing from 7 to 5 V	ΔG_v	typ.	3	dB


7Z52382
frequency response curve of tape-recorder
pre-amplifier during recording
gain at 1kHz is 64dB
ΔGv
(dB)
20
15
10
5
0
−5
−10
typ
10
2
5
10²
2
5
10³
2
5
10⁴
2
5
10⁵
f (Hz)


7Z52383
frequency response curve of tape-recorder
pre-amplifier during play-back
gain at 1kHz is 64dB
ΔGv
(dB)
20
15
10
5
0
−5
−10
typ
10
2
5
10²
2
5
10³
2
5
10⁴
2
5
10⁵
f (Hz)

INTEGRATED MOST AMPLIFIER

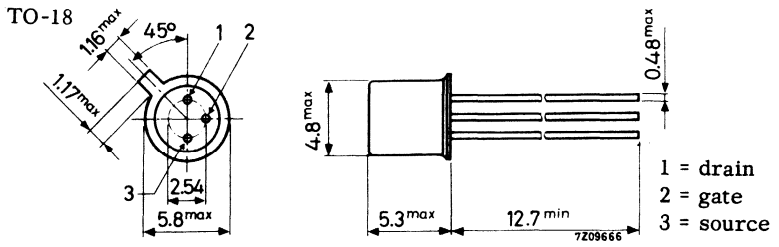
The TAA320 is a silicon monolithic integrated circuit, consisting of a MOS transistor and an n-p-n transistor in a TO-18 metal envelope.
The device is primarily intended for audio amplifiers with a very high input resistance (e.g. for crystal pick-ups).
Besides this application the TAA320 is also suitable for other applications where a high input resistance is required, like impedance converters, timing circuits, microphone-amplifiers, etc.

QUICK REFERENCE DATA				
Drain-source voltage (V_{GS} = 0)	$-V_{DSS}$	max.	20	V
Drain current	$-I_D$	max.	25	mA
Gate-source voltage $-I_D$ = 10 mA; $-V_{DS}$ = 10 V	$-V_{GS}$	typ.	11	V
Gate-source resistance $-V_{GS}$ up to 20 V; T_j up to 125 °C	r_{GS}	>	100	GΩ
Transfer admittance at f = 1 kHz $-I_D$ = 10 mA; $-V_{DS}$ = 10 V	$\|y_{fs}\|$	typ.	75	$m\Omega^{-1}$

PACKAGE OUTLINE

Dimensions in mm

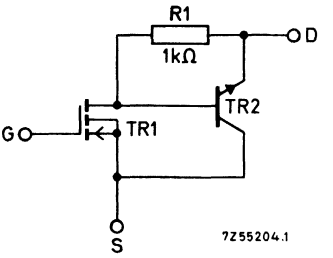
TO-18



Source connected to the case

Accessories available: 56246, 56263

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages				
Drain-source voltage (V_{GS} = 0)	$-V_{DSS}$	max.	20	V
Gate-source voltage (I_D = 0)	$-V_{GSO}$	max.	20	V
Non repetitive peak gate-source voltage ($t \leq 10$ ms)	$-V_{GSM}$	max.	100	V
Current				
Drain current	$-I_D$	max.	25	mA
Power dissipation				
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	200	mW
Temperatures				
Storage temperature	T_{stg}	−55 to +125		°C
Operating ambient temperature (see derating curve on page 8)	T_{amb}	−20 to +125		°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	0.5	°C/mW

CHARACTERISTICS T_j = 25 °C unless otherwise specified

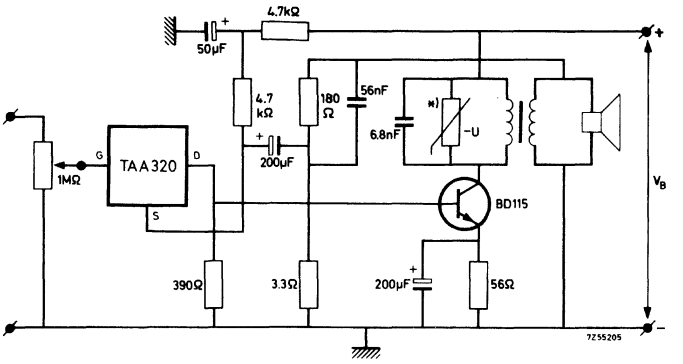
Drain current				
$-V_{DS}$ = 20 V; V_{GS} = 0	$-I_{DSS}$	typ. <	5 1	nA μA
Gate-source voltage [1]				
$-I_D$ = 10 mA; $-V_{DS}$ = 10 V	$-V_{GS}$	typ. 9 to	11 14	V V
Gate-source resistance				
$-V_{GS}$ up to 20 V; T_j up to 125 °C	r_{GS}	>	100	GΩ
Equivalent noise voltage				
$-I_D$ = 10 mA; $-V_{DS}$ = 10 V B = 50 Hz to 15 kHz	v_n	typ.	25	μV
y parameters at f = 1 kHz				
$-I_D$ = 10 mA; $-V_{DS}$ = 10 V				
Transfer admittance	$\|y_{fs}\|$	typ. 40 to 120	75 	$m\Omega^{-1}$ $m\Omega^{-1}$
Input capacitance	C_{is}	typ.	8	pF
Feedback capacitance	$-C_{rs}$	typ.	1.5	pF
Output conductance	g_{os}	typ.	0.65	$m\Omega^{-1}$

NOTE

To exclude the possibility of damage to the gate oxide layer by an electrostatic charge building up on the high resistance gate electrode, the leads of the device have been short circuited by a clip. The clip has been arranged so that it need not be removed until the device has been mounted in the circuit.

1) $-V_{GS}$ decreases about 6 mV/°C with increasing ambient temperature at a constant $-I_D$.

APPLICATION INFORMATION 2 W audio amplifier with TAA320 and BD115



* The voltage dependent resistor (2322 552 03381) suppresses voltage transients that might otherwise exceed the safe operating limits of the BD115.

Supply voltage	V_B	=	100	V
Collector current of BD115	I_C	typ.	50	mA
Drain current of TAA320	$-I_D$	typ.	9.5	mA
Primary d.c. resistance of output transformer			140	Ω
Primary inductance of output transformer			2.7	H
A.C. collector load for BD115			1.8	kΩ

Performance at f = 1 kHz; feedback = 16 dB

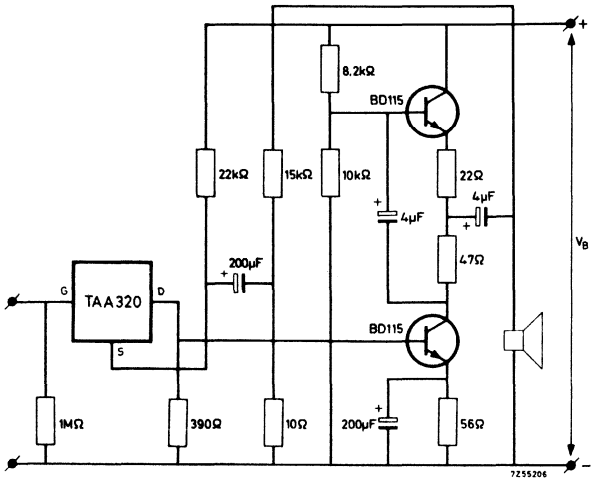
Output power at d_{tot} = 10% (on primary of the output transformer)	P_o	typ.	2.6	W
Input voltage for P_o = 50 mW	$V_{i(rms)}$	typ.	13.5	mV
Input voltage for P_o = 2 W	$V_{i(rms)}$	typ.	86	mV
Total distortion at P_o = 2 W	d_{tot}	typ.	3.6	%
Minimum frequency response (−3 dB)		60 Hz to 20		kHz
Signal-noise ratio at P_o = 2 W		typ.	73	dB

Mounting instruction for BD115

Proper continuous operation is ensured up to T_{amb} = 50 °C, provided the BD115 is directly mounted on a 1.5 mm blackened Al. heatsink of 30 cm^2 with a clamping washer of type 56218.
If the transistor is mounted on a heatsink with a mica washer, the heatsink should have an area of 50 cm^2.
Recommended diameter of hole in heatsink: 7.7 mm.

APPLICATION INFORMATION (continued)

4 W audio amplifier with TAA320 and 2 transistors of type BD115.

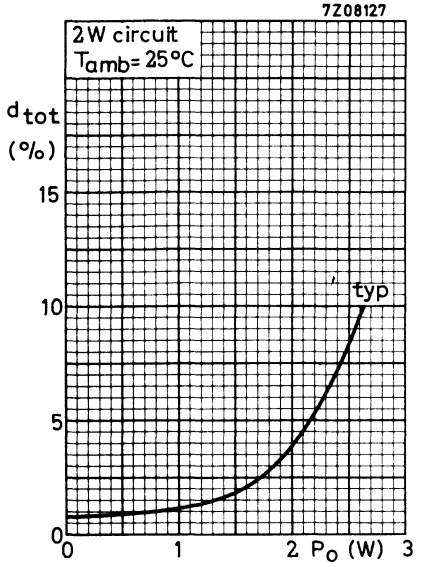


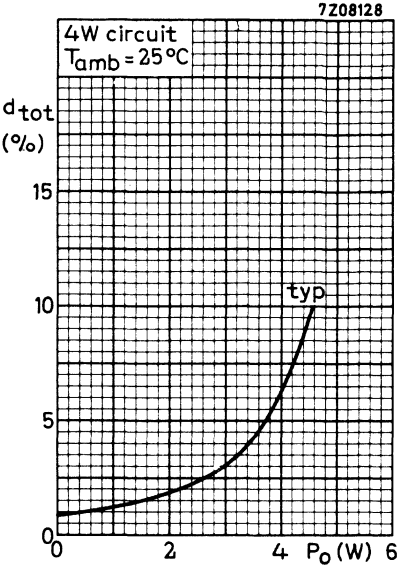
Supply voltage	V_B	=	200	V
Collector current of a BD115	I_C	typ.	52	mA
Drain current of TAA320	$-I_D$	typ.	8.6	mA

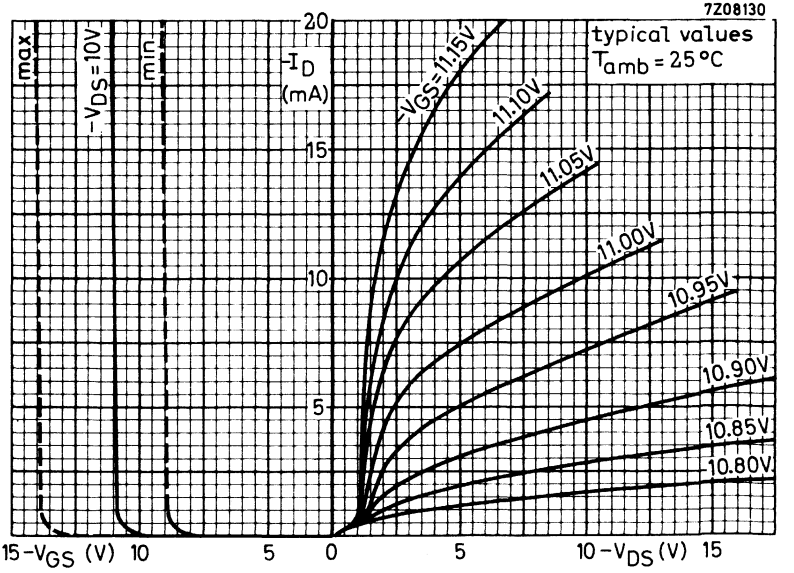
Performance at f = 1 kHz; feedback = 12 dB

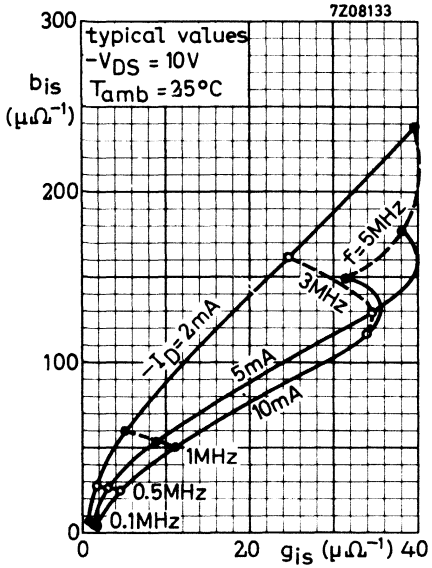
Output power at d_{tot} = 10%	P_o	typ.	4.5	W
Input voltage for P_o = 50 mW	$V_{i(rms)}$	typ.	7.5	mV
Input voltage for P_o = 4 W	$V_{i(rms)}$	typ.	67	mV
Total distortion at P_o = 4 W	d_{tot}	typ.	6	%
Minimum frequency response (-3 dB)		50 Hz to	20	kHz
Signal-noise ratio at P_o = 4 W		typ.	73	dB

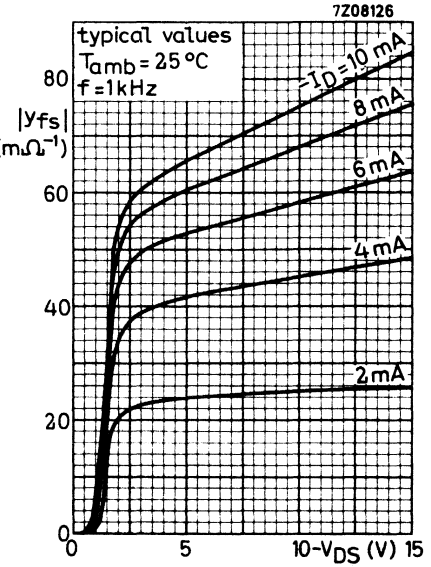
Mounting instruction for BD115 see page 4

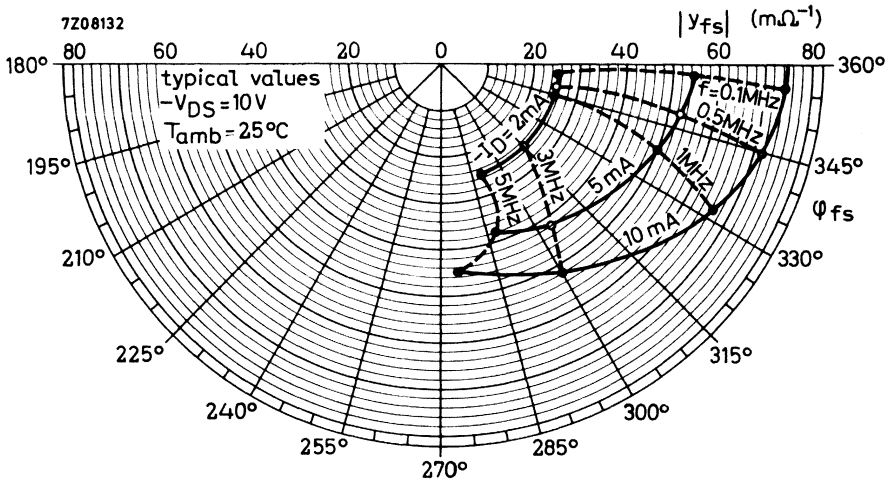

7Z08127
2W circuit
Tamb = 25°C
dtot
(%)
15
10
5
0
typ
0
1
2 Po (W) 3

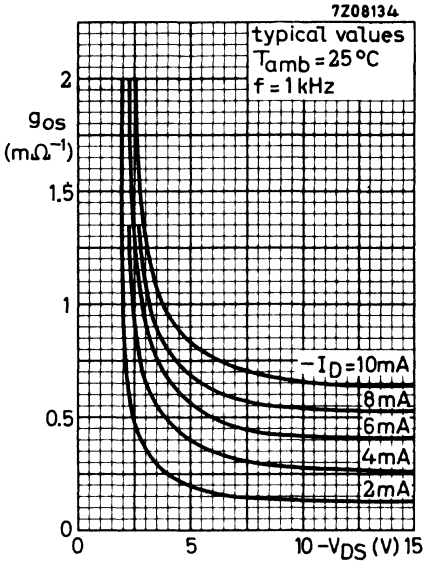

7Z08128
4W circuit
Tamb = 25°C
dtot
(%)
15
10
5
0
typ
0
2
4 Po (W) 6

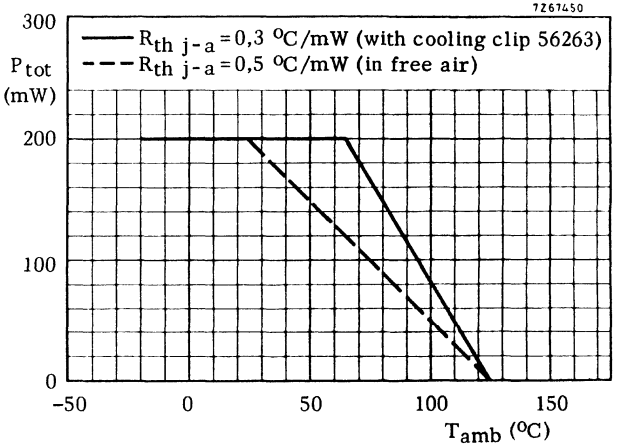

7Z08130
typical values
Tamb = 25°C
max
-VDS = 10V
min
-ID
(mA)
20
15
10
5
-VGS = 11.15V
11.10V
11.05V
11.00V
10.95V
10.90V
10.85V
10.80V
15 -VGS (V) 10
5
0
5
10 -VDS (V) 15

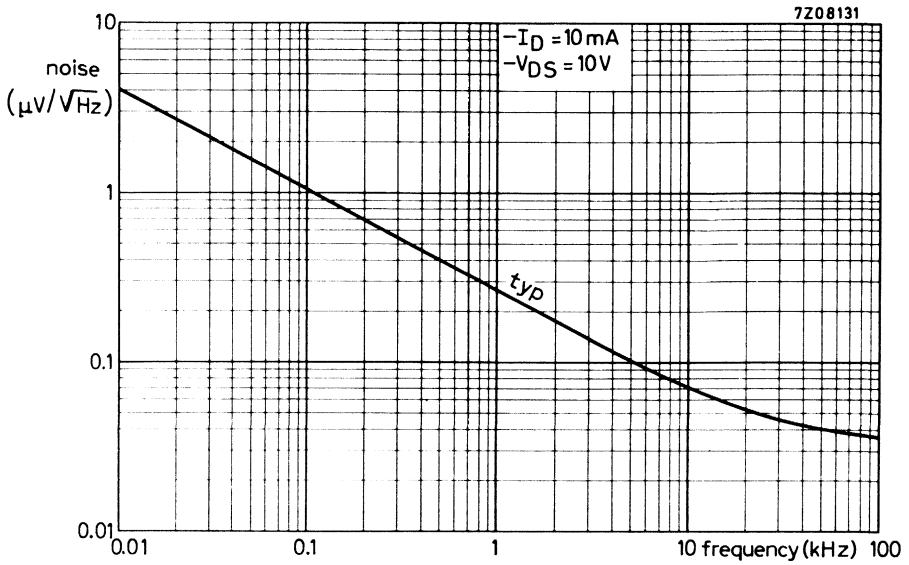

7Z08133
typical values
$-V_{DS}$ = 10V
T_{amb} = 25°C
b_{is} ($\mu\Omega^{-1}$)
g_{is} ($\mu\Omega^{-1}$)
$-I_D$ = 2mA
5mA
10mA
f = 5MHz
3MHz
1MHz
0.5MHz
0.1MHz


7Z08126
typical values
T_{amb} = 25°C
f = 1kHz
$|y_{fs}|$ ($m\Omega^{-1}$)
$10-V_{DS}$ (V)
$-I_D$ = 10 mA
8 mA
6 mA
4 mA
2mA


7Z08132
$|y_{fs}|$ ($m\Omega^{-1}$)
typical values
$-V_{DS}$ = 10V
T_{amb} = 25°C
$-I_D$ = 2mA
5mA
10 mA
f = 0.1MHz
0.5MHz
1MHz
3MHz
5MHz
φ_{fs}


7Z08134
typical values
T_{amb} = 25 °C
f = 1 kHz
g_{os}
(mΩ^{-1})
2
1.5
1
0.5
0
0
5
10
15
$-V_{DS}$ (V)
$-I_D$=10mA
8mA
6mA
4mA
2mA


7Z67450
$R_{th\ j-a}$ = 0,3 °C/mW (with cooling clip 56263)
$R_{th\ j-a}$ = 0,5 °C/mW (in free air)
P_{tot}
(mW)
300
200
100
0
-50
0
50
100
150
T_{amb} (°C)


7Z08131
10
noise
(μV/√Hz)
1
0.1
0.01
$-I_D = 10\,mA$
$-V_{DS} = 10\,V$
typ
0.01
0.1
1
10 frequency (kHz) 100

INTEGRATED MOST LEVEL SENSOR

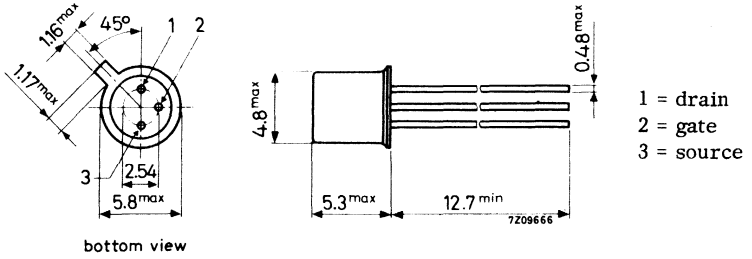
The TAA320A is a silicon monolithic integrated circuit, consisting of a p-channel enhancement type MOS transistor and an n-p-n transistor, in a TO-18 metal envelope. The device is intended for level sensors with a very high input resistance (e.g. timing circuits, thermostats, liquid level sensors, flame control circuits).

QUICK REFERENCE DATA					
Drain-source voltage (V_{GS} = 0)		$-V_{DSS}$	max.	20	V
Drain current		$-I_D$	max.	60	mA
Gate-source voltage [1])					
$-I_D$ = 10 mA; $-V_{DS}$ = 10 V	group 1:	$-V_{GS}$	typ.	10,6	V
			10,0 to	11,2	V
	group 2:	$-V_{GS}$	typ.	11,3	V
			10,7 to	11,9	V
	group 3:	$-V_{GS}$	typ.	12,0	V
			11,4 to	12,6	V
	group 4:	$-V_{GS}$	typ.	12,7	V
			12,1 to	13,3	V
Gate cut-off current at T_{amb} = 25 °C					
$-V_{GS}$ = 20 V; I_D = 0		$-I_{GSO}$	typ.	1	pA
$-V_{GS}$ = 20 V; V_{DS} = 0		$-I_{GSS}$	typ.	1	pA

PACKAGE OUTLINE

Dimensions in mm

TO-18

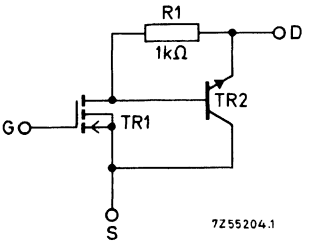


source connected to the case

Accessories available on request: 56246; 56263

[1]) For explanation of the group codefication see note b on page 3.

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

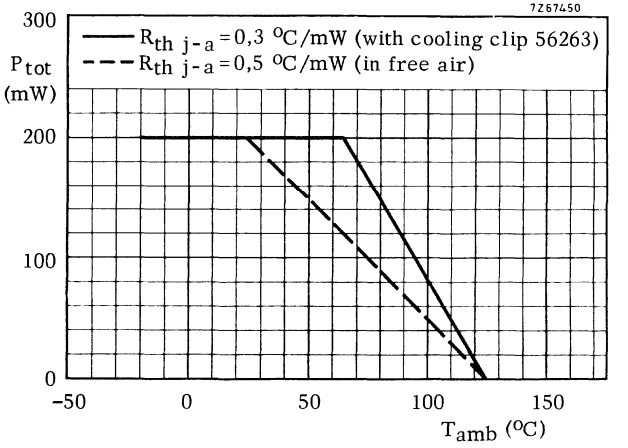
Drain-source voltage (V_{GS} = 0)	$-V_{DSS}$	max.	20	V
Gate-source voltage (I_D = 0)	$-V_{GSO}$	max.	20	V
Non-repetitive peak gate-source voltage (t ≤10 ms)	$\pm V_{GSM}$	max.	100	V

Current

Drain current	$-I_D$	max.	60	mA
Peak drain current (t < 200 ms; δ 0,001)	$-I_{DM}$	max.	100	mA

Temperatures

Storage temperature	T_{stg}	−65 to +125	°C
Operating ambient temperature (see curve below)	T_{amb}	−20 to +125	°C



CHARACTERISTICS T_j = 25 °C unless otherwise specified

Drain current					
$-V_{DS}$ = 20 V; V_{GS} = 0		$-I_{DSS}$	typ. <	5 1	nA µA
Drain-source voltage [1]					
$-I_D$ = 10 mA; $-V_{GS}$ = 20 V		$-V_{DS}$	<	1	V
$-I_D$ = 60 mA; $-V_{GS}$ = 20 V		$-V_{DS}$	<	1,5	V
Gate-source voltage (see note b)					
$-I_D$ = 10 mA; $-V_{DS}$ = 10 V	group 1:	$-V_{GS}$	typ. 10,0 to	10,6 11,2	V V
	group 2:	$-V_{GS}$	typ. 10,7 to	11,3 11,9	V V
	group 3:	$-V_{GS}$	typ. 11,4 to	12,0 12,6	V V
	group 4:	$-V_{GS}$	typ. 12,1 to	12,7 13,3	V V
Gate cut-off current					
$-V_{GS}$ = 20 V; I_D = 0		$-I_{GSO}$	typ.	1	pA [2]
$-V_{GS}$ = 20 V; V_{DS} = 0		$-I_{GSS}$	typ.	1	pA [2]

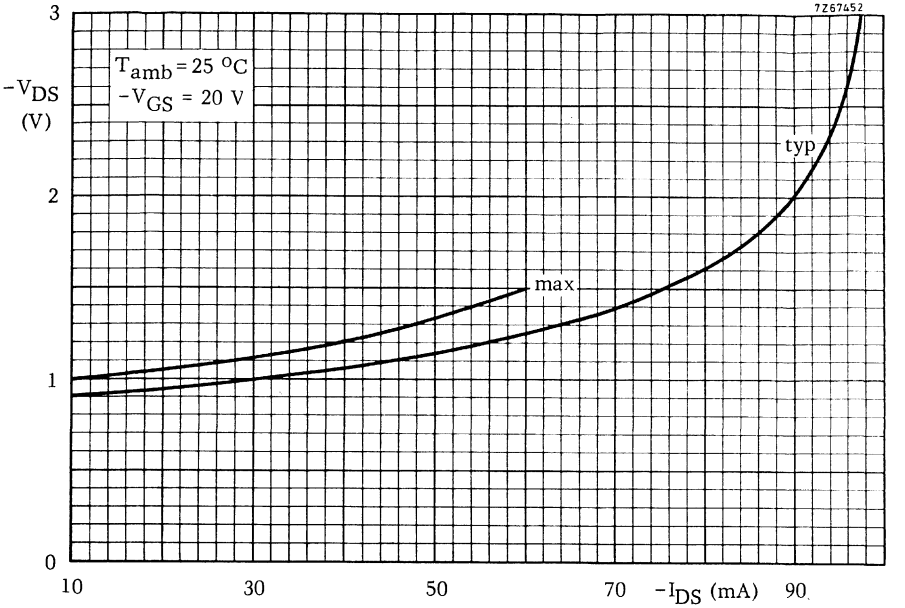
NOTES

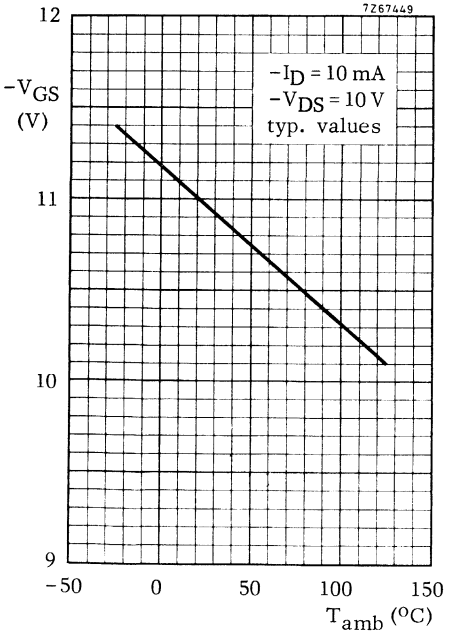
a. The leads are short-circuited by a clip to protect the oxide layer against damage due to accumulation (or build-up) of electrostatic charge on the high resistance gate electrode. The clip should not be removed until after the device is mounted.

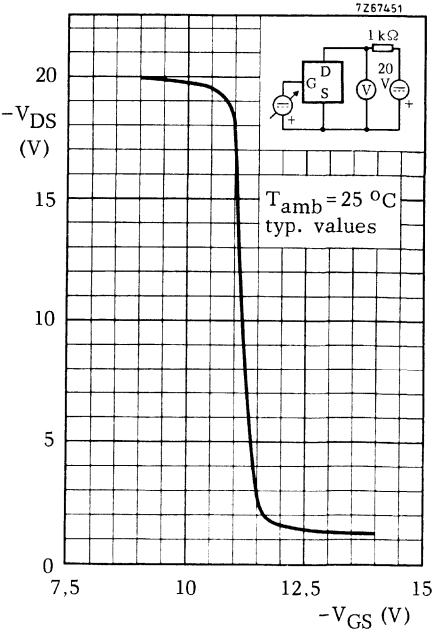
b. As a service to the customer the $-V_{GS}$ group to which a device belongs is identified by a numerical suffix (1, 2, 3 or 4), however, individual groups cannot be ordered separately.

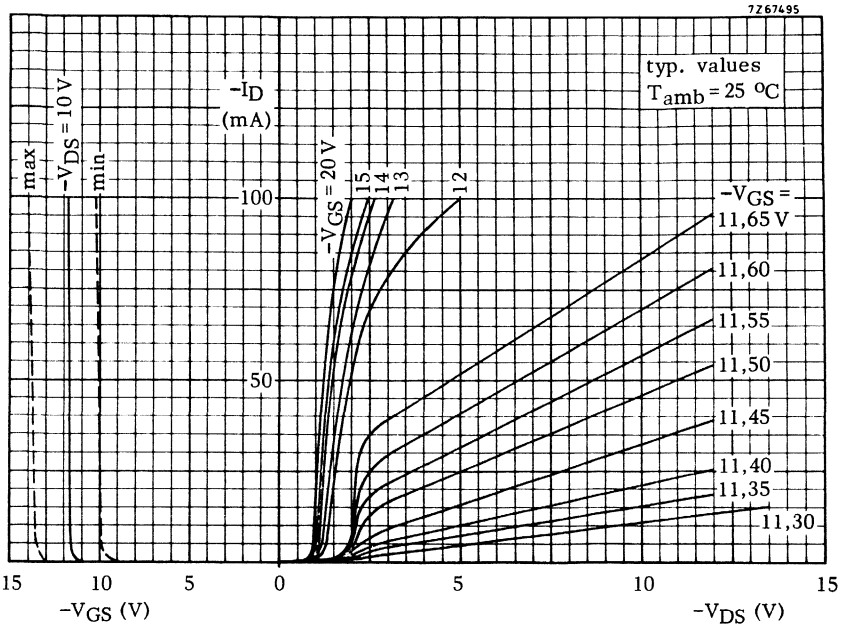
1. See also upper graph on page 4.

2. Being dependent on handling and ambient humidity, the quoted value applies only up to the time of shipping.
Efficient drying treatment is advised before the device is mounted, provided the application requires this low current.


7Z67452
T_{amb} = 25 °C
$-V_{GS}$ = 20 V
typ
max
$-V_{DS}$ (V)
3
2
1
0
10
30
50
70
90
$-I_{DS}$ (mA)


7Z67449
$-I_D$ = 10 mA
$-V_{DS}$ = 10 V
typ. values
$-V_{GS}$ (V)
12
11
10
9
−50
0
50
100
150
T_{amb} (°C)


7Z67451
1 kΩ
D
G
S
20 V
T_{amb} = 25 °C
typ. values
$-V_{DS}$ (V)
20
15
10
5
0
7,5
10
12,5
15
$-V_{GS}$ (V)


7Z67495
typ. values
T_{amb} = 25 °C
$-I_D$ (mA)
100
50
max
min
$-V_{DS}$ = 10 V
$-V_{GS}$ = 20 V
15
14
13
12
$-V_{GS}$ =
11,65 V
11,60
11,55
11,50
11,45
11,40
11,35
11,30
15
10
5
0
5
10
15
$-V_{GS}$ (V)
$-V_{DS}$ (V)

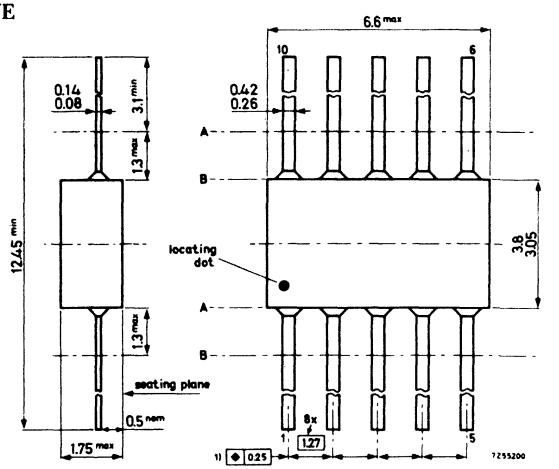
HEARING-AID AMPLIFIER

Integrated monolithic a.f. amplifier for use in hearing aids. The collector current of the class A output transistor can be determined externally, making the circuit suitable for a wide range of output powers at a low current consumption. Provision is made for the use of peak-clipping and frequency compensation circuits, and special measures have been taken to minimize the influence of temperature and supply voltage variations.

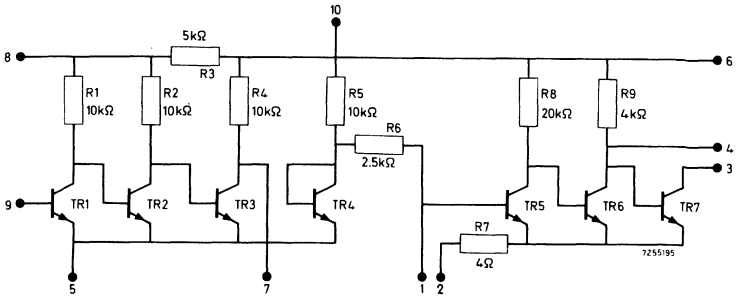
QUICK REFERENCE DATA				
Supply voltage	V_B	nom.	1.3	V
Transducer gain	G_{tr}	typ.	90	dB
Output power at d_{tot} = 10%	P_o	typ.	1.5	mW
Saturation voltage of TR7 at I_C = 5 mA; V_{6-2} = 1.3 V	V_{3-2sat}	<	300	mV
Current consumption of all stages except output stage	I	typ.	0.35	mA
Noise figure	F	typ.	3	dB

PACKAGE OUTLINE

TO-89



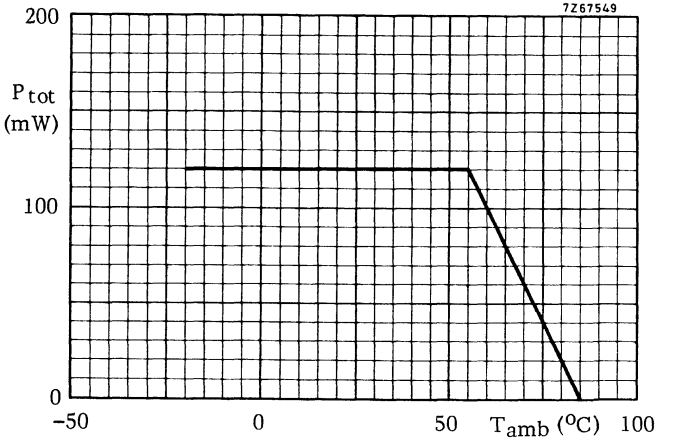
CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages	V_{6-2}	max.	5	V
	V_{3-2}	max.	5	V
	V_{8-2}	max.	5	V
	V_{5-9}	max.	5	V
Currents	I_2	max.	20	mA
	I_3	max.	20	mA

Maximum allowable total power dissipation versus ambient temperature



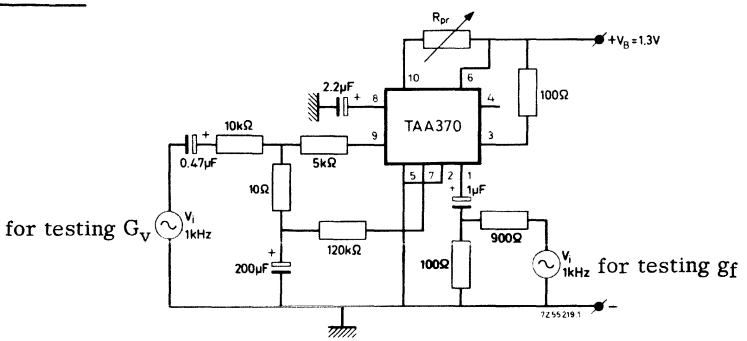
→ Temperatures

Storage temperature	T_{stg}	−55 to +125	°C
Operating ambient temperature (see derating curve above)	T_{amb}	−20 to +85	°C

CHARACTERISTICS (see also test circuit) $T_{amb} = 25\ ^{o}C$

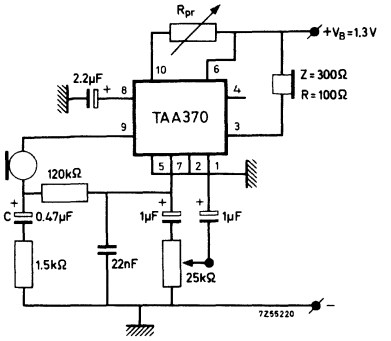
Supply voltage	V_B	nom.	1.3	V
Voltage gain of first 3 transistors (pin 9 to 7)	G_v	>	60	dB
Transconductance of last 3 transistors (pin 1 to 3)	g_f	200 to 280		$m\Omega^{-1}$
Saturation voltage of last transistor (TR7) at $I_C = 5$ mA; $V_{6-2} = 1.3$ V	$V_{3-2\,sat}$	<	300	mV
Current consumption of all stages except output stage	I	typ. <	0.35 0.5	mA mA
Noise figure $R_S = 5$ kΩ; B = 400 to 3200 Hz	F	typ. <	3 6	dB dB

Test circuit



APPLICATION INFORMATION

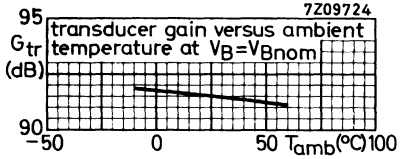
The TAA370 in a 1.5 mW amplifier

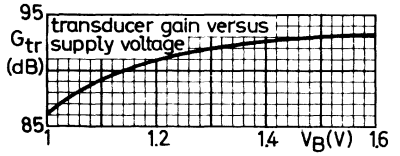


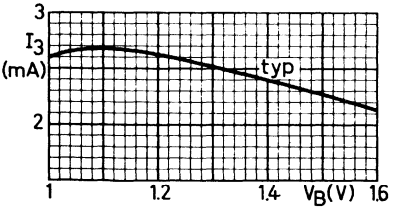
I_3 = 2.5 mA

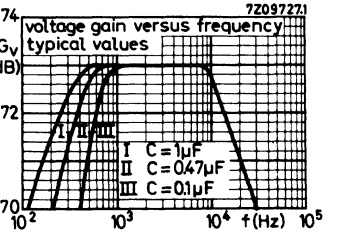
I_{tot} = 2.85 mA

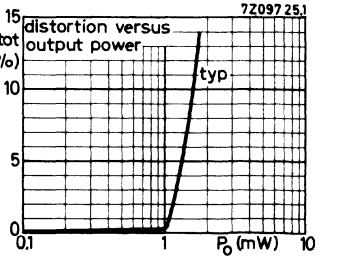
R_{pr} = 4 kΩ











LOW FREQUENCY AMPLIFIER

The TAA480 is a silicon monolithic integrated a.f. amplifier suitable for use as channel amplifier in telephone carrier equipment. The accurate amplification and input and output impedances required for this application make the use of low tolerance resistors imperative. Therefore only the transistors and diodes have been integrated.

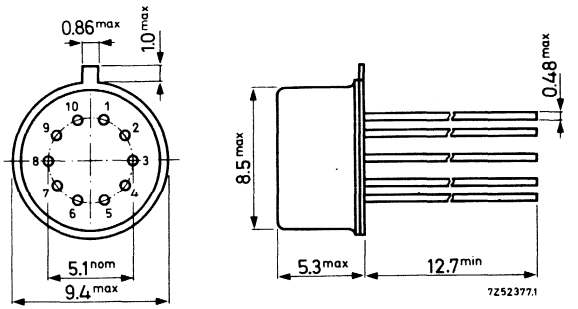
Owing to the push-pull configuration of the output stage no d.c. current will flow through the output transformer. This makes considerable savings possible.

QUICK REFERENCE DATA				
(see test circuit on page 4)				
Supply voltage	V_B	nom.	20	V
Voltage gain	G_v	typ.	15	dB
Output voltage at d_{tot} = 1%	$V_{o(rms)}$	min.	4	V

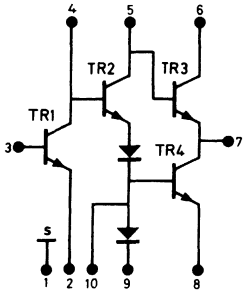
PACKAGE OUTLINE

Dimensions in mm

TO-74 reduced height



CIRCUIT DIAGRAM



RATINGS (Limiting values) [1])

Voltages	V_{4-3}	max.	25	V
	V_{4-2}	max.	25	V
	V_{5-4}	max.	25	V
	V_{5-10}	max.	25	V
	V_{6-5}	max.	25	V
	V_{6-7}	max.	25	V
	V_{7-10}	max.	25	V
	V_{7-8}	max.	25	V
	V_{10-1}	max.	25	V
	V_{4-1}	max.	25	V
	V_{5-1}	max.	25	V
	V_{6-1}	max.	25	V
	V_{7-1}	max.	25	V
	V_{2-3}	max.	5	V
	V_{10-4}	max.	10	V
	V_{7-5}	max.	5	V
	V_{8-10}	max.	5	V
Currents	I_4	max.	10	mA
	I_5	max.	10	mA
	I_6	max.	10	mA
Total power dissipation up to $T_{amb} = 75\ ^{o}C$	P_{tot}	max.	200	mW
Temperatures				
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		−5 to +75	°C

1) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.

CHARACTERISTICS at T_{amb} = 25 °C

TRANSISTOR TR1

D.C. current gain

I_C = 0.2 mA; V_{CB} = 5 V	h_{FE}	typ.	125	
		50 to	300	

TRANSISTORS TR3 and TR4

Saturation voltage

I_C = 10 mA; I_B = 1 mA	V_{CEsat}	typ.	260	mV
		<	600	mV

EACH TRANSISTOR

Collector cut-off current

I_E = 0; V_{CB} = 10 V	I_{CBO}	<	100	nA

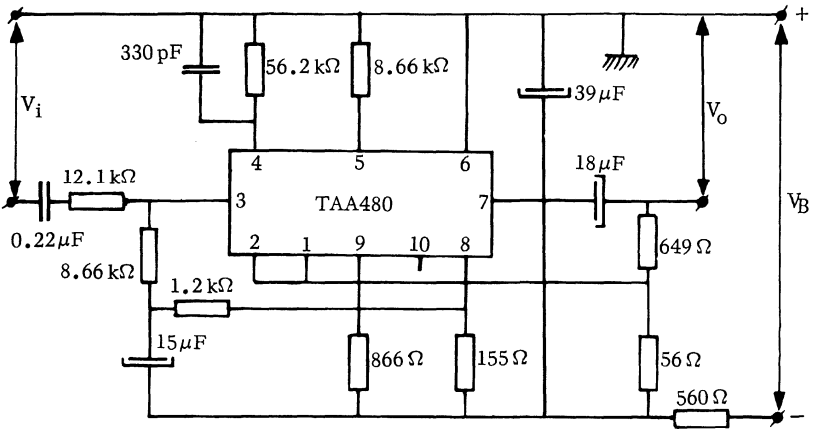
Collector-substrate leakage current

V_{CS} = 10 V	I_{CSO}	<	100	nA

PERFORMANCE in recommended test circuit

Supply voltage	V_B	nom.	20	V
Output voltage at d_{tot} = 1%	$V_{o(rms)}$	>	4	V
Distortion at P_o = 4.5 mW	d_{tot}	<	0.1	%
Input voltage at P_o = 4.5 mW	$V_{i(rms)}$	typ.	310	mV
D.C. collector voltage				
of TR4	V_{7-6}	typ.	7.8	V
		6.3 to	9.4	V
Total current drain	I_{tot}	typ.	5.2	mA
		4.75 to	5.6	mA

Test circuit:



VOLTAGE STABILIZER

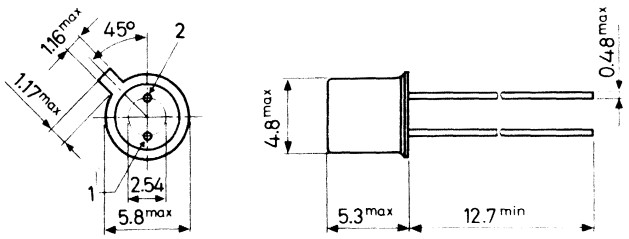
The TAA550 is an integrated monolithic voltage stabilizer, especially designed to provide the supply voltage for variable capacitance diodes in television tuners independent of supply voltage and temperature variations.
The TAA550 is supplied in 3 voltage groups, identified by a coloured dot on the envelope:

Stabilized voltage V_{12}: 30 to 32 V red dot
32 to 34 V yellow dot
34 to 35 V green dot

QUICK REFERENCE DATA			
Supply current	I_1	typ. 5	mA
Stabilized voltage	V_{12}	30 to 35	V
Differential internal resistance	r_{12}	typ. 10	Ω

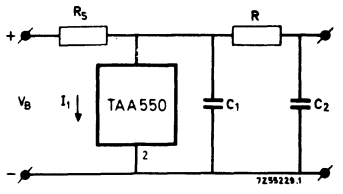
PACKAGE OUTLINE Dimensions in mm

TO-18; 2 pins



pin 1 connected to the case

RECOMMENDED CIRCUIT

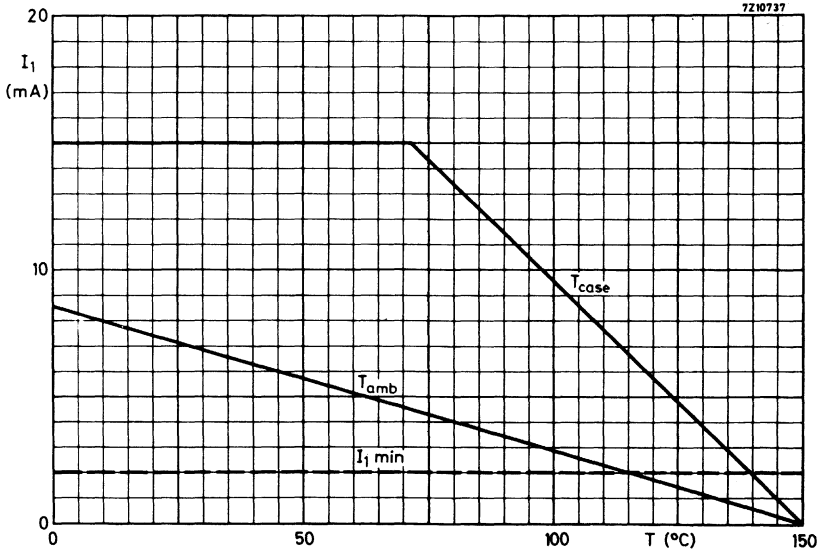


$V_B >> V_{12}$
I_1 typ. 5 mA
$R \geq 22\ \Omega$
C_1 = 300 to 4700 pF

C_2: to be connected if decoupling for low frequent noise is necessary
In practice values up to 10 μF are used.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Maximum allowable supply current versus temperature



Temperatures

Storage temperature	T_{stg}	-55 to +150	°C
Operating ambient temperature	T_{amb}	-20 to +150	°C

CHARACTERISTICS

Recommended supply current	I_1	>	2	mA
		typ.	5	mA
Stabilized voltage	V_{12}		30 to 35	V
Differential internal resistance at f = 1 kHz I_1 = 5 mA	r_{12}	typ.	10	Ω
		<	25	Ω
Temperature coefficient at T_{amb} = 10 to 50 °C	$\frac{\Delta V_{12}}{\Delta T_{amb}}$	typ.	-0,13	mV/°C
			-3,1 to +1,55	mV/°C

SYNCHRONOUS DEMODULATOR FOR COLOUR DIFFERENCE DRIVE

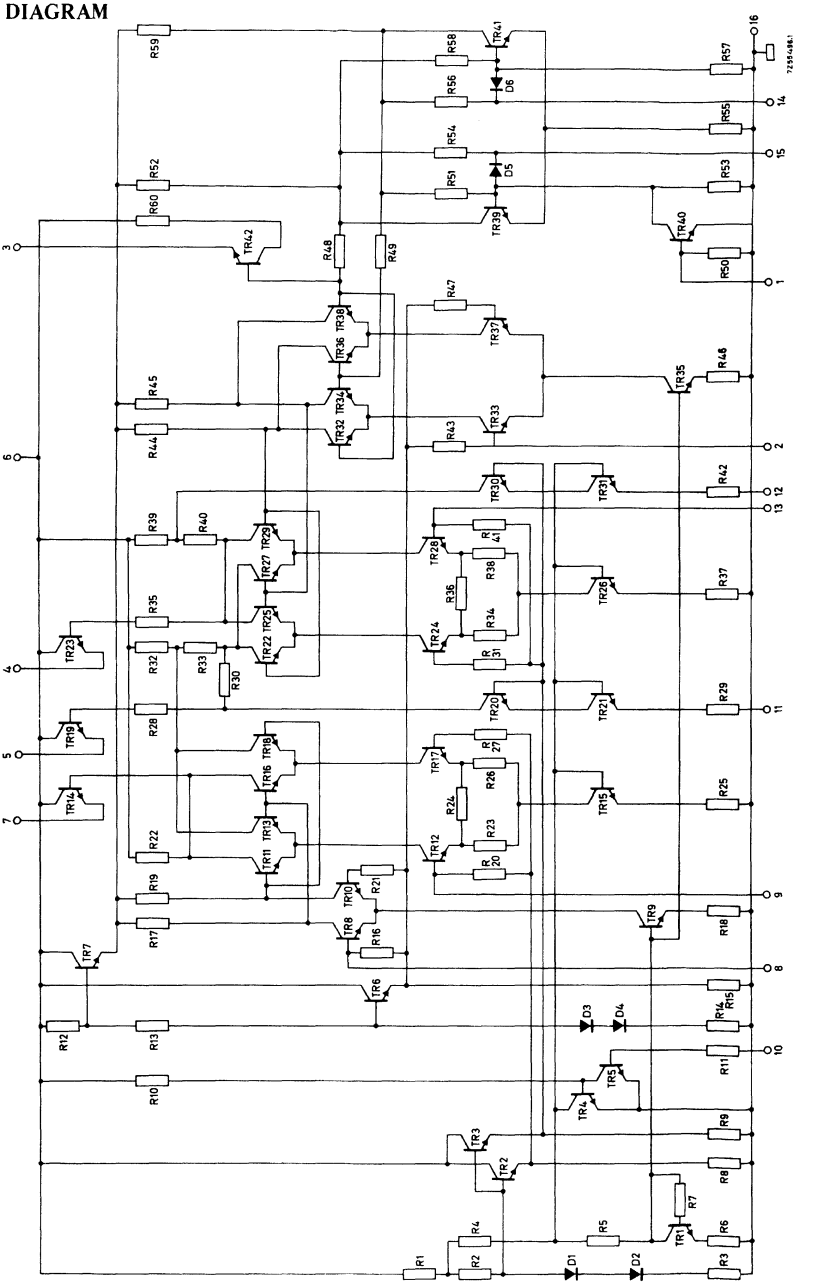
The TAA630 is a synchronous demodulator for direct drive of colour difference output stages with clamping circuits in television sets. The circuit consists of 2 amplifying synchronous demodulators for the B-Y and R-Y signals, a matrix, a PAL switch, a bistable multivibrator and colour killer switch.

QUICK REFERENCE DATA				
Supply voltage	V_{6-16}	nom.	12	V
Ambient temperature	T_{amb}		25	°C
Gain of R-Y demodulator	$G_{v(R-Y)}$	typ.	6	
Gain of B-Y demodulator	$G_{v(B-Y)}$	typ.	10.7	
Input impedance of B-Y and R-Y channel	$\lvert Z_{9-16} \rvert$	typ.	1	kΩ
	$\lvert Z_{13-16} \rvert$	typ.	1	kΩ
Output impedance of R-Y, B-Y and G-Y channel	$\lvert Z_{4-16} \rvert$	≤	100	Ω
	$\lvert Z_{5-16} \rvert$	≤	100	Ω
	$\lvert Z_{7-16} \rvert$	≤	100	Ω

PACKAGE OUTLINE

TAA630S: 16 lead plastic dual in-line (See General Section)
TAA630T: 16 lead plastic quadruple in-line (See General Section)

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

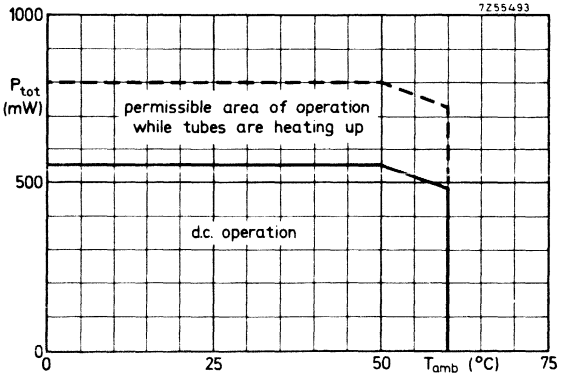
Supply voltage	V_{6-16}	max.	13.2	V
	V_{6-16}	max.	16	V [1]
Pin No. 1 voltage	$-V_{1-16}$	max.	5	V

Currents

Pin No. 4 current	I_4	max.	5	mA
Pin No. 5 current	I_5	max.	5	mA
Pin No. 7 current	I_7	max.	5	mA
Pin No. 1 current	I_1	max.	1	mA

Power dissipation

Total power dissipation	P_{tot}	max.	550	mW
	P_{tot}	max.	800	mW [1]



Temperatures

Storage temperature	T_{stg}	−20 to +125 °C
Operating ambient temperature	T_{amb}	−20 to +60 °C

[1]) Permissible while tubes are heating up.

CHARACTERISTICS at $V_{6-16} = 12$ V; $V_{10-16} = 0.9$ V; $T_{amb} = 25\ ^{o}C$

Gain of colour difference signals

→ $V_{i(p-p)} = 50$ mV; f = 4.4 MHz	$G_{v(R-Y)}$	typ.	6	[1]
G-Y = 0.51 (R-Y) −0.19 (B-Y)	$\frac{G_{v(B-Y)}}{G_{v(R-Y)}}$	typ.	1.78	

Input impedance of R-Y and B-Y channels

$V_{i(rms)} = 20$ mV (sine wave): f = 4.4 MHz

at input F_{R-Y}; input resistance	R_{13-16}	≥	800	Ω
input capacitance	C_{13-16}	≤	10	pF
at input F_{B-Y}; input resistance	R_{9-16}	≥	800	Ω
input capacitance	C_{9-16}	≤	10	pF

Input impedance of reference inputs

$V_{i(rms)} = 400$ mV (sine wave): f = 4.4 MHz

at reference R-Y input	$\lvert Z_{2-16}\rvert$		660 to 1250	Ω
at reference B-Y input	$\lvert Z_{8-16}\rvert$		660 to 1250	Ω

Colour difference output voltages

(peak to peak values)	output R-Y	$V_{4-16(p-p)}$	≤	3.2	V [2][3]
	output B-Y	$V_{7-16(p-p)}$	≤	4.0	V [2][3]
	output G-Y	$V_{5-10(p-p)}$	≤	1.8	V [2][3]

Output impedances of R-Y, B-Y and G-Y channels

at output R-Y	$\lvert Z_{4-16}\rvert$	≤	100	Ω
at output B-Y	$\lvert Z_{7-16}\rvert$	≤	100	Ω
at output G-Y	$\lvert Z_{5-16}\rvert$	≤	100	Ω

[1]) Ratio of peak to peak values of input and output voltage measured in test circuit on page 6.

$G_{v(R-Y)} = \frac{V_{4-16}}{V_{13-16}}$; $G_{v(B-Y)} = \frac{V_{7-16}}{V_{9-16}}$

[2]) Linearity of gain ≥ 0.7

[3]) Measured in the test circuit on page 6.

CHARACTERISTICS (continued)

Colour difference d.c. output voltages			
at output B-Y	V_{7-16}	typ. 7.4 V	[1]
at output R-Y	adjustable to the same level as V_{7-16}		[1][2]
at output G-Y	adjustable to the same level as V_{7-16}		[1][2]
Output voltage; 7.8 kHz (square wave; peak to peak value)			
R_{load} = 4.7 kΩ; $V_{14-16} = V_{15-16}$ = 2.5 to 5 V	$V_{3-16(p-p)}$	typ. 2.5 V	←
Input voltages			
Reference voltages (peak to peak value)			
at reference R-Y	$V_{2-16(p-p)}$	typ. 1 V	[3]
at reference B-Y	$V_{8-16(p-p)}$	typ. 1 V	[3]
Horizontal deflection pulses (peak value)			
at pin No. 14	$-V_{14-16M}$	2.5 to 5 V	
at pin No. 15	$-V_{15-16M}$	2.5 to 5 V	
Identification signal (peak to peak value)	$V_{1-16(p-p)}$	2 to 6 V	
ident "on"	V_{1-16}	≥ 0.75 V	←
	I_1	≥ 80 μA	←
ident "off"	V_{1-16}	≤ 0.4 V	←
Colour killer voltage and current			
colour "on"	V_{10-16}	≥ 0.9 V	
colour "off"	V_{10-16}	≤ 0.3 V	

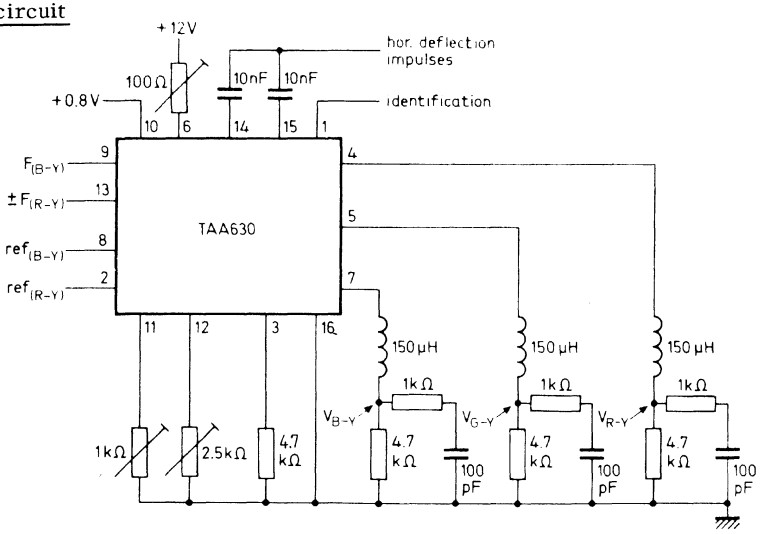
[1]) Measured in the test circuit on page 6.

[2]) To be adjusted with a variable voltage ($V \leq 1.2$ V) or with resistors connected between pin 11 and pin 16 for G-Y and between pin 12 and pin 16 for R-Y.

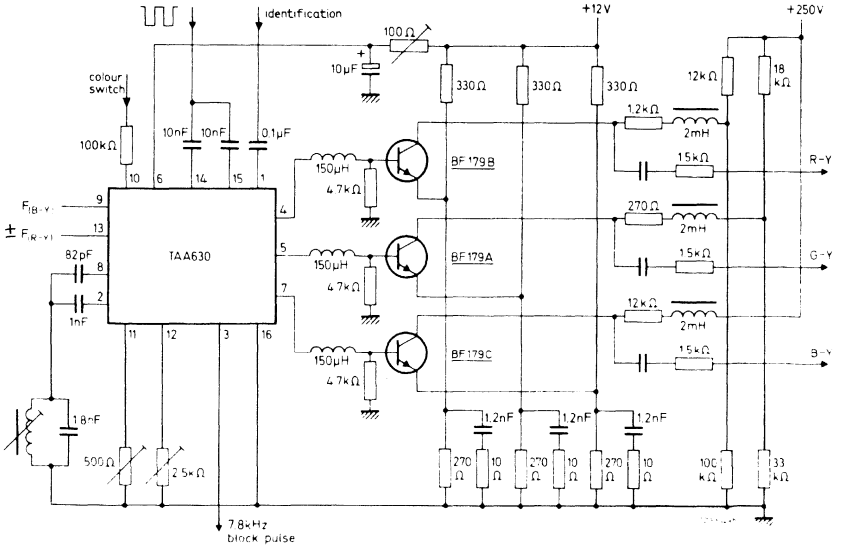
[3]) Permissible range 0.5 to 2 V. ←

CHARACTERISTICS (continued)

Test circuit



APPLICATION INFORMATION



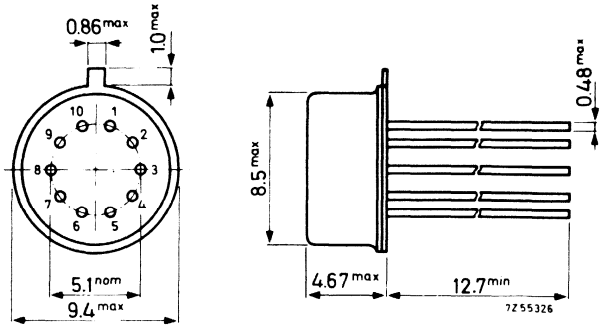
TRIPLE AMPLIFIER FOR ACTIVE FILTERS

The TAA960 consists of three identical general-purpose amplifiers integrated in a single silicon chip. The amplifiers can be used **separately** or can be cascaded to give a voltage gain of 117 dB. One of the amplifiers has an additional emitter-follower stage. The TAA960 is very suitable for use in an active RC band-pass filter with Q up to 60.

QUICK REFERENCE DATA				
Supply voltage	V_{3-10}	nom.	6	V
Supply current	I_3	typ.	2	mA
Transfer admittance (each amplifier)	$\|y_{fs}\|$	typ.	9.5	$m\Omega^{-1}$
Voltage gain (each amplifier)	G_v	typ.	39	dB
Input resistance (on pins 1, 7 and 8)	R_i	>	25	kΩ
Output resistance (on pins 2, 5 and 6)	R_o	typ.	9	kΩ
(on pin 4)	R_o	typ.	500	Ω
Q factor (in typical RC filter)	Q	typ.	45	

PACKAGE OUTLINE TO-74; reduced height

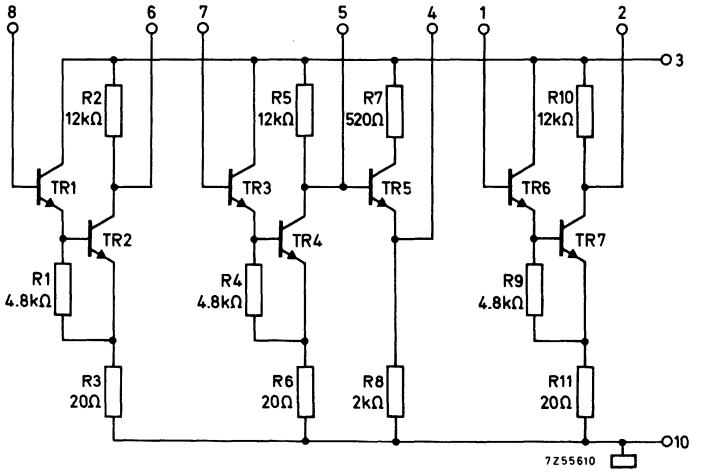
Dimensions in mm



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages with respect to pin 10				
Supply voltage [1])	V_3	max.	10	V
Input voltage	V_8, V_7, V_1	max.	4	V
Output voltage	V_6, V_5, V_4, V_2	max.	10	V
Currents				
Input current	I_8, I_7, I_1	max.	50	μA
Total power dissipation	P_{tot}	max.	250	mW
Temperatures				
Storage temperature	T_{stg}	−65 to +125		°C
Operating ambient temperature	T_{amb}	−55 to + 65		°C

CIRCUIT DIAGRAM



[1]) With lower d.c. potential on all other terminals.

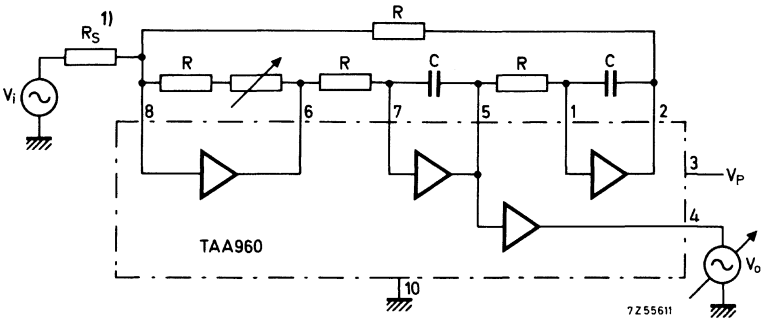
CHARACTERISTICS at $V_3 = 6$ V; $T_{amb} = 25\ ^{o}C$ unless otherwise specified.

Supply current [1]	I_3		1.5 to 2.5	mA
		typ.	2.0	mA
Supply current [1] at $V_3 = 10$ V	I_3		1.5 to 3.8	mA
		typ.	2.6	mA
Voltage gain (each amplifier)	G_v		60 to 150	
		typ.	90	
Input resistance (each amplifier)	R_i	>	25	kΩ
Output resistance on terminals 2, 5 and 6	R_o	>	8	kΩ
		typ.	9	kΩ
on terminals 4	R_o		135 to 750	Ω

[1]) Terminal 8 connected to terminal 6
" 7 " " " 5
" 1 " " " 2

APPLICATION INFORMATION

Active RC filter for frequencies up to 150 kHz



R = 10 kΩ

Frequency	f	typ.	$\frac{1}{2\pi RC}$	
Supply voltage	V_P	typ.	6	V
Filter performance				
at T_{amb} = 25 °C	Q	typ.	40 to 55	
			45	
at T_{amb} = −30 to +65 °C	Q		35 to 55	
Input voltage	V_i	typ.	400	mV
Output voltage	V_o	typ.	400	mV
Distortion at V_o = 350 mV	d_{tot}	typ.	2	%
S/N ratio at V_o = 400 mV	S/N	>	50	dB
Input resistor 1)	R_S	typ.	470	kΩ

1) Value of input resistor to be determined for $\frac{V_o}{V_i}$ = 0.90 to 1.1.

MICROPHONE AMPLIFIER

The TAA970 is a monolithic integrated microphone amplifier for use in telephone systems. It is compatible with both piezo-electric and dynamic microphones of suitable impedance and sensitivity.

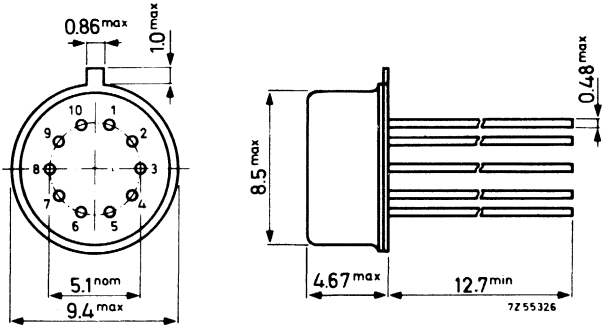
Special features are:

- almost constant voltage gain and d.c. voltage drop with supply current variations of 10 to 100 mA
- output voltage before limiting: 1 V (r.m.s. value)
- operation is independent of supply voltage polarity
- gain can be set to either of two values
- only one external capacitor required
- output impedance determined by internal feed back

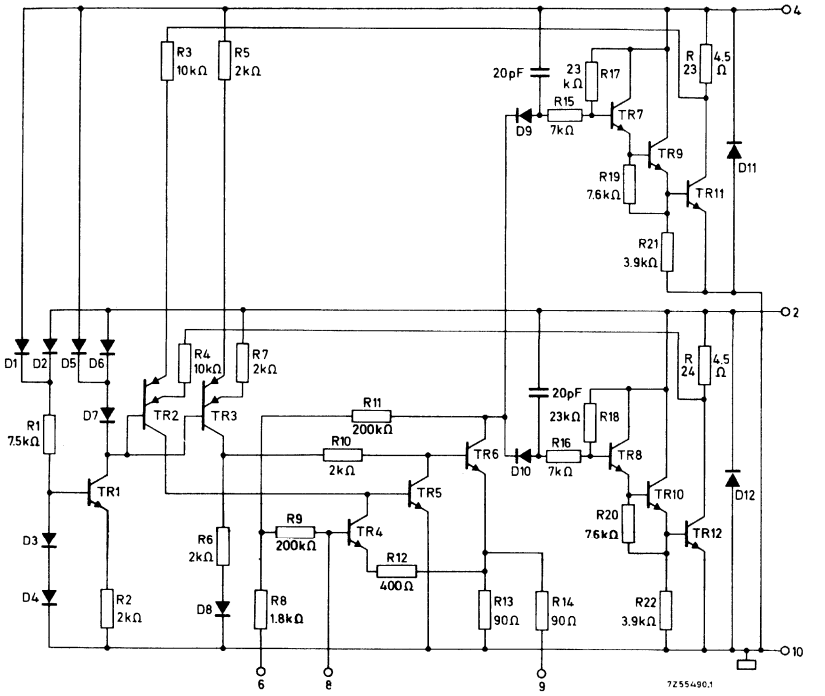
QUICK REFERENCE DATA			
Supply current	$\pm I_2$	10 to 100	mA
Supply voltage drop	$\pm V_{2-4}$	typ. 4.5	V
Voltage gain			
pin 9 not connected	G_v	typ. 150	
pin 9 connected to pin 10	G_v	typ. 210	
Output impedance			
pin 9 not connected	R_o	typ. 60	Ω
pin 9 connected to pin 10	R_o	typ. 100	Ω

PACKAGE OUTLINE

TO-74 (reduced height) Dimensions in mm



CIRCUIT DIAGRAM



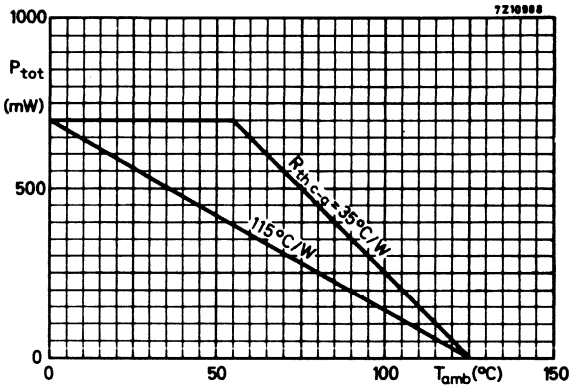
RATINGS Limiting values in accordance to the Absolute Maximum System (IEC 134).

Currents

Supply current (d.c.)	I_2	-100 to +100		mA
A.C. component of supply current (peak value)	I_{2m}	max.	100	mA
Pin No.6 current	I_6	max.	100	μA
Pin No.8 current	I_8	max.	100	μA

Power dissipation

Total power dissipation	P_{tot}	max.	700	mW



Temperatures

Storage temperature	T_{stg}	-55 to +125		°C
Operating ambient temperature	T_{amb}	-35 to + 75		°C

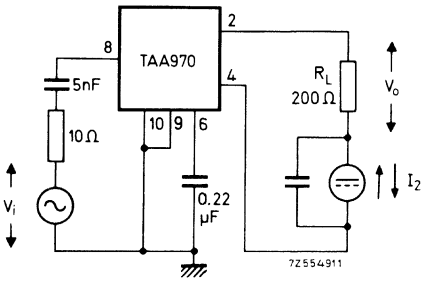
THERMAL RESISTANCE

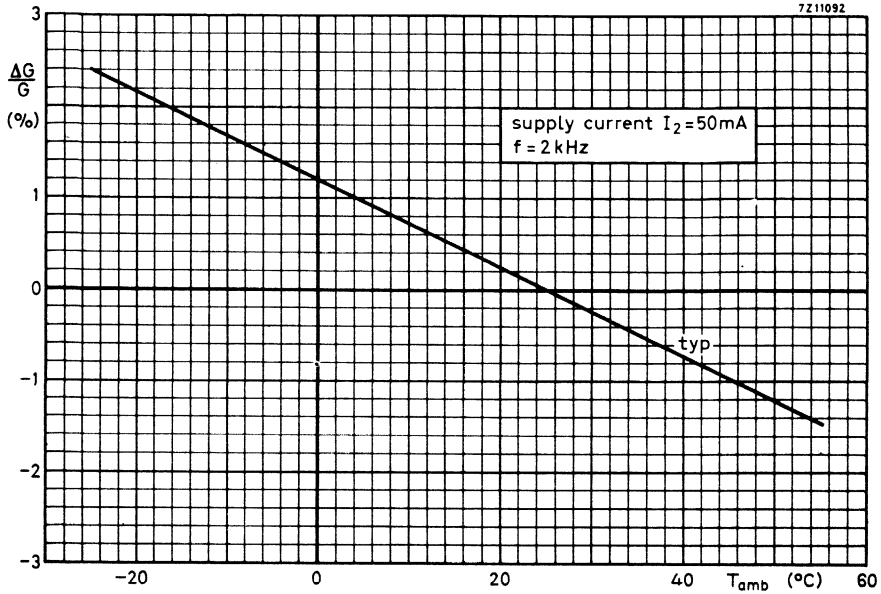
From junction to case	$R_{th\,j-c}$	=	65	°C/W

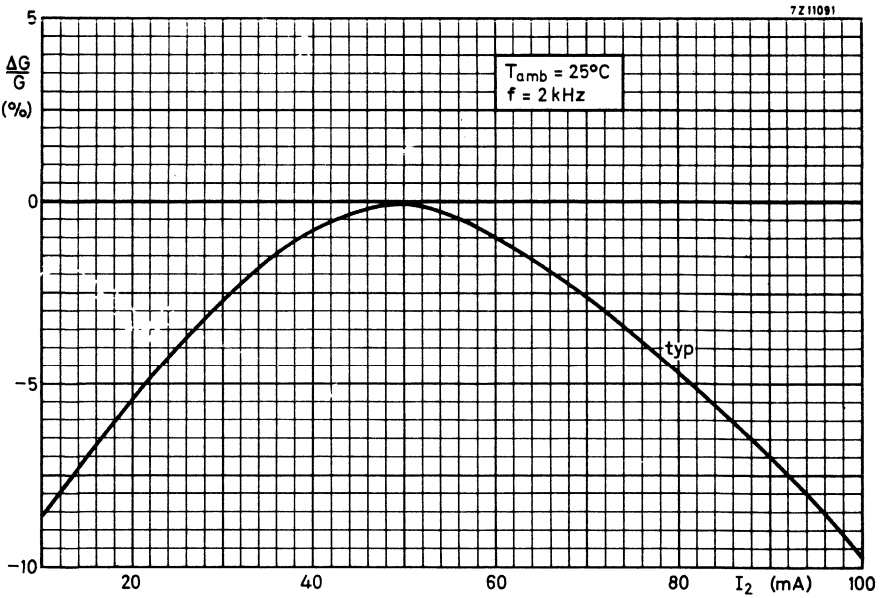
CHARACTERISTICS at R_L = 200Ω; f = 2 kHz; T_{amb} = 25 °C unless otherwise specified. (see test circuit below).

Supply voltage drop at $R_{th\ j-a}$ = 100 °C/W				
$\pm I_2$ = 10 mA	$\pm V_{2-4}$	typ.	4.5	V
		<	5.4	V
$\pm I_2$ = 50 mA	$\pm V_{2-4}$	<	5.8	V
$\pm I_2$ = 100 mA	$\pm V_{2-4}$	<	6.0	V
Voltage gain				
pin 9 not connected; $\pm I_2$ = 10 mA	G_v	typ.	140	
		105 to	165	
pin 9 not connected; $\pm I_2$ = 50 mA	G_v	typ.	150	
		125 to	165	
pin 9 connected to pin 10; $\pm I_2$ = 10 mA	G_v	typ.	200	
		150 to	230	
pin 9 connected to pin 10; $\pm I_2$ = 50 mA	G_v	typ.	210	
		180 to	230	
Change of voltage gain				
due to change of supply voltage polarity	ΔG_v	<	10	%
Gain reduction at f = 300 Hz (with respect to f = 2 kHz)	ΔG_v	typ.	1	dB
		<	3	dB
Output impedance at $\pm I_2$ = 50 mA				
pin 9 not connected	R_o	typ.	60	Ω
pin 9 connected to pin 10	R_o	typ.	100	Ω
Noise output voltage at B = 0.3 kHz to 4 kHz				
pin 9 not connected	$V_{n(rms)}$	<	1	mV
pin 9 connected to pin 10	$V_{n(rms)}$	<	1.3	mV
Output voltage				
I_2 = 25 mA; d_{tot} = 5%	V_o	>	0.85	V
		typ.	1.0	V

Test circuit:




7Z11092
3
ΔG/G (%)
1
0
-1
-2
-3
supply current I_2=50mA
f = 2kHz
typ
-20
0
20
40
T_{amb} (°C)
60


7Z11091
5
ΔG/G (%)
0
-5
-10
T_{amb} = 25°C
f = 2kHz
typ
20
40
60
80
I_2 (mA)
100

RING (DE)MODULATOR FOR TELEPHONY AND INDUSTRIAL EQUIPMENT

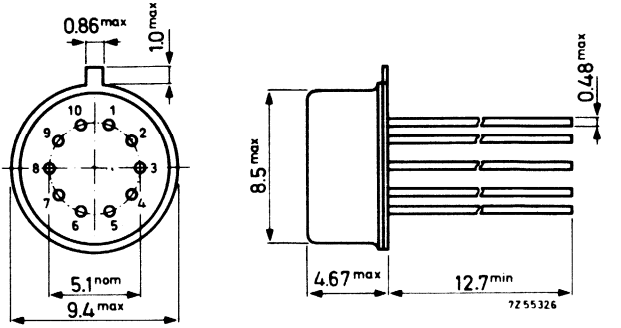
The TAB101 is a monolithic integrated circuit comprising a 4-transistor modulator and demodulator circuit. The circuit being made on a single crystal ensures a great similarity in characteristics of the transistors and optimal tracking of their parameters with temperature variations. Consequently, the TAB101 gives a better balancing and therefore less carrier leakage than a conventional circuit. The use of transistors instead of diodes provides a better isolation between input and output circuits.

QUICK REFERENCE DATA				
Collector cut-off current V_{CB} = 5 V; T_{amb} = 25 °C	I_{CBO}	<	100	nA
Base-emitter voltage differences between transistors 1, 2, 3, 4 V_{CB} = 5 V; $-I_E$ = 150 μA	$\lvert V_{BE1}-V_{BE2} \rvert$ $\lvert V_{BE3}-V_{BE4} \rvert$	< <	5 5	mV mV
Common-base current gain differences between transistors 1, 2, 3, 4 V_{CB} = 5 V; $-I_E$ = 150 μA	$\lvert h_{FB1}-h_{FB2} \rvert$ $\lvert h_{FB3}-h_{FB4} \rvert$	< 0.008 < 0.008		

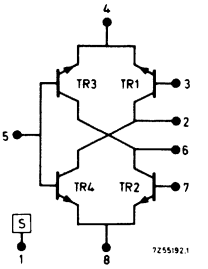
PACKAGE OUTLINE

Dimensions in mm

TO-74 (reduced height)



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages (each transistor)

Collector-base voltage (open emitter)	V_{CBO}	max.	10	V
Emitter-base voltage (open collector)	V_{EBO}	max.	5	V
Collector-substrate voltage	V_{CS}	max.	12	V

Currents (each transistor)

Collector current	I_C	max.	10	mA

Power dissipation (4 transistors)

Total power dissipation up to T_{amb} = 100 °C	P_{tot}	max.	100	mW

Temperatures

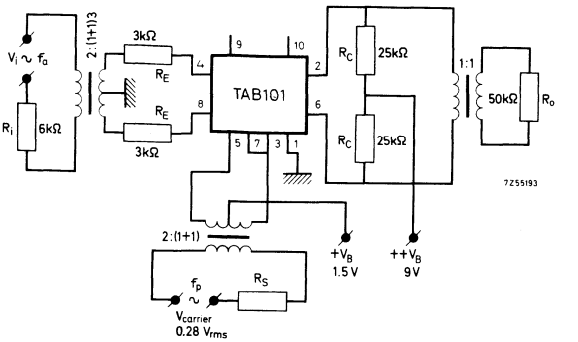
Storage temperature	T_{stg}	−35 to +125		°C
Operating ambient temperature	T_{amb}	−25 to +100		°C

CHARACTERISTICS (each transistor) T_{amb} = 25 °C

Collector cut-off current				
I_E = 0; V_{CB} = 5 V	I_{CBO}	typ. <	5 100	nA nA
Collector-substrate leakage current				
V_{CS} = 9.5 V	I_{CS}	typ. <	5 100	nA nA
Emitter cut-off current				
I_C = 0; V_{EB} = 1 V	I_{EBO}	typ. <	5 100	nA nA
Break down voltages				
I_E = 0; I_C = 10 μA	$V_{(BR)CBO}$	>	10	V
I_B = 0; I_C = 10 μA	$V_{(BR)CEO}$	>	9	V
$-I_S$ = 10 μA	$V_{(BR)CS}$	>	12	V
I_C = 0; I_E = 200 μA	$V_{(BR)EBO}$	>	5	V
D.C. current gain				
I_C = 150 μA; V_{CE} = 5 V	h_{FE}	> typ.	20 75	
Spot noise figure at f = 1 kHz				
$-I_E$ = 150 μA; V_{CB} = 5 V				
R_S = 1 kΩ; Bandwidth: 200 Hz		typ.	6	dB
Base-emitter voltage difference				
between transistors TR1 and TR2 at				
$-I_{E1} = -I_{E2}$ = 150 μA; $V_{CB1} = V_{CB2}$ = 5 V	$\lvert V_{BE1}-V_{BE2}\rvert$	typ. <	2 5	mV mV
between transistors TR3 and TR4 at				
$-I_{E3} = -I_{E4}$ = 150 μA; $V_{CB3} = V_{CB4}$ = 5 V	$\lvert V_{BE3}-V_{BE4}\rvert$	typ. <	2 5	mV mV
Current amplification factor difference				
between transistors TR1 and TR2 at				
$-I_{E1} = -I_{E2}$ = 150 μA; $V_{CB1} = V_{CB2}$ = 5 V	$\lvert h_{FB1}-h_{FB2}\rvert$	typ. <	0.002 0.008	
between transistors TR3 and TR4 at				
$-I_{E3} = -I_{E4}$ = 150 μA; $V_{CB3} = V_{CB4}$ = 5 V	$\lvert h_{FB3}-h_{FB4}\rvert$	typ. <	0.002 0.008	

APPLICATION INFORMATION

Telephony carriers ring modulator



Performance at T_{amb} = 25 °C

Conversion gain at f_a = 1 kHz,

V_i = 0.4 V; f_p = 34 kHz	G_c	typ.	−0.75	dB
Carrier leakage power in R_o at f_p = 34 kHz	P_{oc}	typ.	3	nW

OPERATIONAL AMPLIFIER

The TBA221 is a silicon monolythic integrated operational amplifier for use at temperatures from 0 to 70 °C. Special features are:

- no frequency compensation required
- continuous short circuit protection
- offset voltage adjustable to zero
- large input voltage range
- low power consumption
- no latch up

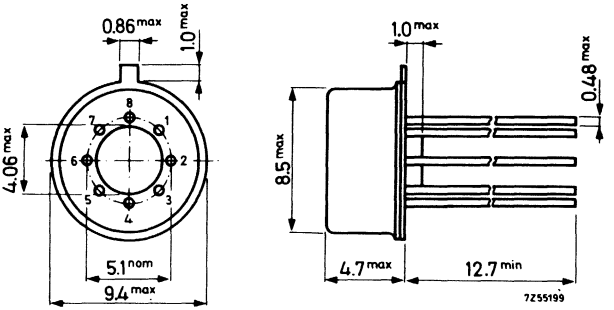
The TBA221 is equivalent to 741C.

QUICK REFERENCE DATA				
Positive supply voltage	V_P		15	V
Negative supply voltage	$-V_N$		15	V
Characteristics at T_{amb} = 25 °C				
Voltage gain at $R_L \geq 2$ kΩ; $V_o = \pm 10$ V	G_v	typ.	100 000	
Common mode rejection ratio	CMRR	typ.	90	dB
Differential input resistance	R_i	typ.	1	MΩ
Peak output voltage swing at R_L = 10 kΩ	V_{OM}	>	±12	V
Input voltage range	V_i	>	±12	V
Power dissipation	P_{tot}	typ.	50	mW

PACKAGE OUTLINES (for TBA221B and TBA221D see pages 2 and 3)

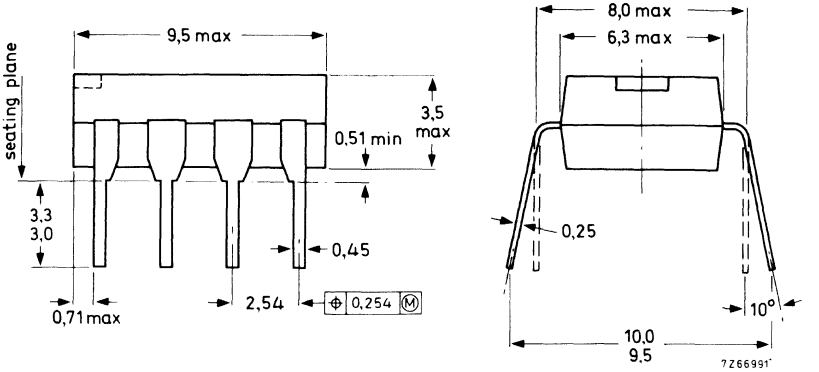
TBA221: TO-99

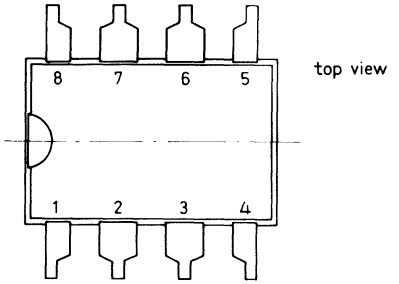
Dimensions in mm



PACKAGE OUTLINES (continued) Dimensions in mm

TBA221B: 8 lead plastic dual in-line

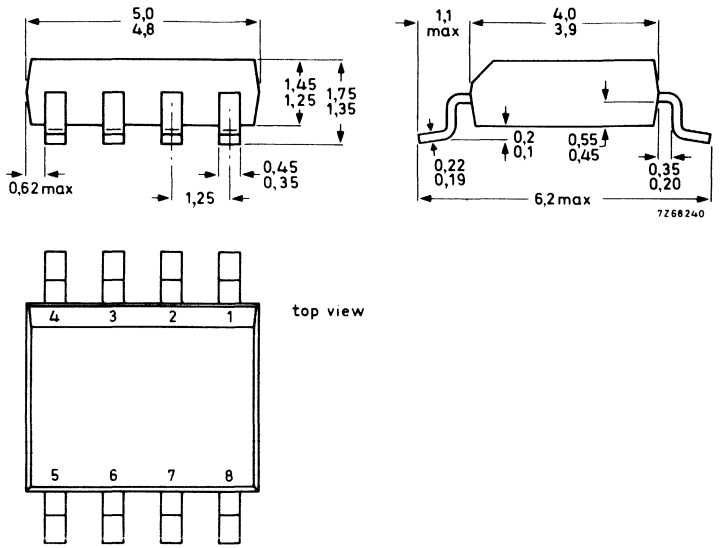




PACKAGE OUTLINES (continued)

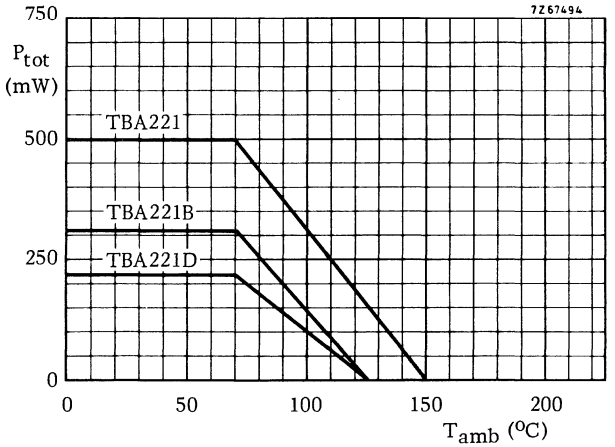
Dimensions in mm

TBA221D: 8 lead plastic envelope (SO-8)



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

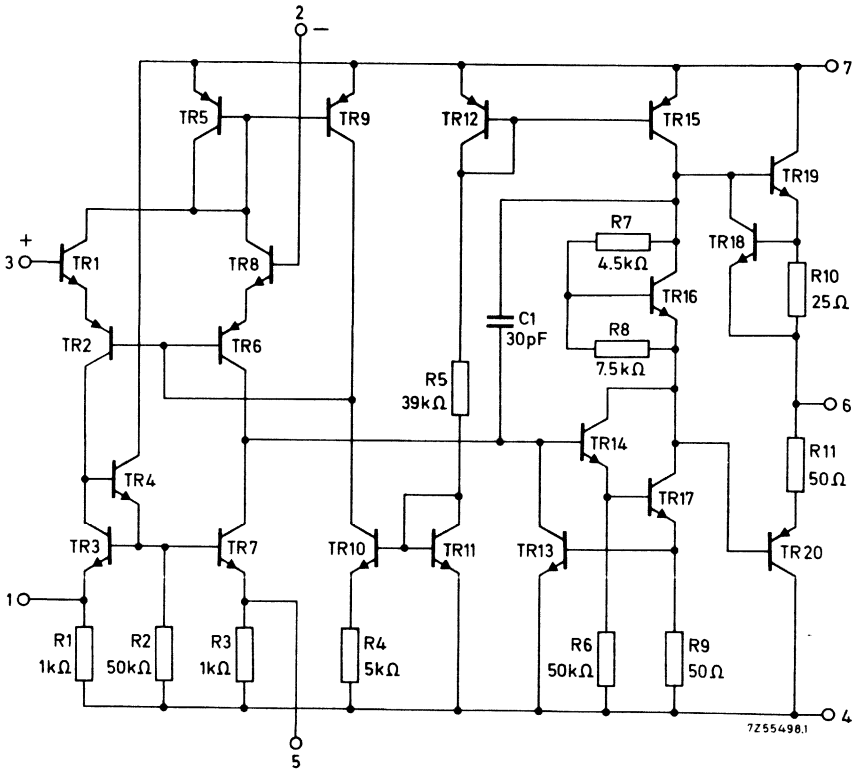
Voltages				
Positive supply voltage	V_P	max.	18	V
Negative supply voltage	$-V_N$	max.	18	V
Common mode input voltage [1])	V_i	max.	±15	V
Differential input voltage	V_{2-3}	max.	±30	V
Power dissipation (see derating curve below)				
TBA221	P_{tot}	max.	500	mW
TBA221B	P_{tot}	max.	310	mW
TBA221D	P_{tot}	max.	220	mW
Output short circuit duration [2])		indefinite		
Temperatures				
Operating ambient temperature see derating curve below	T_{amb}	0 to +70		°C
Storage temperature	T_{stg}	−65 to +150		°C



[1]) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

[2]) Continuous short circuit is allowed to ground or either supply.

CIRCUIT DIAGRAM

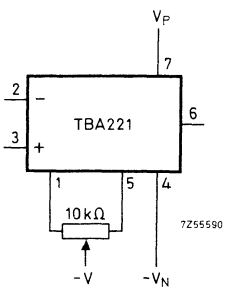


CHARACTERISTICS at V_P = 15 V; $-V_N$ = 15 V; T_{amb} = 25°C unless otherwise specified

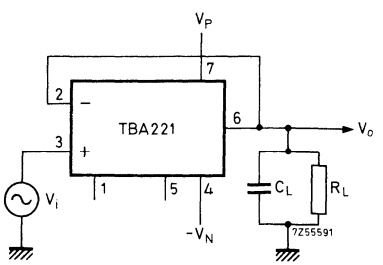
Voltage gain; $R_L \geq 2$ kΩ; $V_O = \pm 10$ V	G_v	>	20 000	
		typ.	100 000	
Input offset voltage; $R_S \leq 10$ kΩ	V_{io}	typ.	2,0	mV
		<	6,0	mV
Input bias current	I_i	typ.	0,2	μA
		<	0,5	μA
Input offset current	I_{io}	typ.	30	nA
		<	0,2	μA
Common mode rejection ratio; $R_S \leq 10$ kΩ	CMRR	>	70	dB
		typ.	90	dB
Input voltage range	V_i	>	±12	V
		typ.	±13	V
Differential input resistance	R_i	>	0,3	MΩ
		typ.	1	MΩ
Supply voltage rejection ratio; $R_S \leq 10$ kΩ	SVRR	typ.	30	μV/V
		<	150	μV/V
Peak output voltage swing at $R_L \geq 10$ kΩ	V_{OM}	>	±12	V
		typ.	±14	V
$R_L \geq 2$ kΩ	V_{OM}	>	±10	V
		typ.	±13	V
Power dissipation at $V_O = 0$	P_{tot}	typ.	50	mW
		<	85	mW
Transient response (unity gain)				
V_i = 20 mV; R_L = 2 kΩ; C_L = 100 pF				
Rise time		typ.	0,3	μs
Overshoot		typ.	5,0	%
Slew rate (unity gain)				
$R_L \geq 2$ kΩ	S	typ.	0,5	V/μs

CHARACTERISTICS at V_P = 15 V; $-V_N$ = 15 V; T_{amb} = 0 to 70 °C unless otherwise specified

Voltage gain; $R_L \geq 2$ kΩ; $V_o = \pm 10$ V	G_V	>	15 000	
Input offset voltage; $R_S \leq 10$ kΩ;	V_{io}	<	7,5	mV
Input bias current	I_i	<	0,8	μA
Input offset current	I_{io}	<	0,3	μA
Peak output voltage swing; $R_L \geq 2$ kΩ	V_{OM}	>	±10	V



Offset voltage zeroing circuit



Transient response test circuit

OPERATIONAL AMPLIFIER

The TBA222 is a silicon monolithic integrated operational amplifier for use at temperatures from −55 to +125 °C. Special features are:

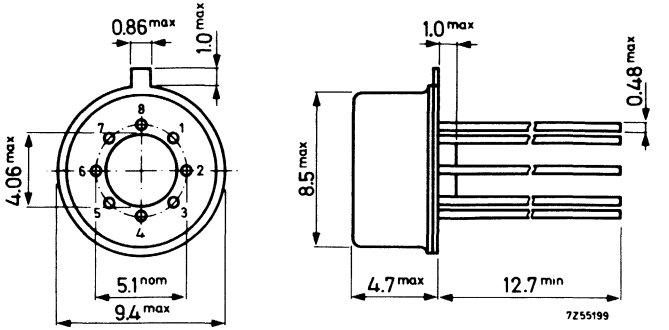
- no frequency compensation required
- continuous short-circuit protection
- offset voltage adjustable to zero
- large input voltage range
- low power consumption
- no latch-up

The TBA222 is equivalent to 741.

QUICK REFERENCE DATA				
Positive supply voltage	V_P		15	V
Negative supply voltage	$-V_N$		15	V
Characteristics at T_{amb} = 25 °C				
Voltage gain at $R_L \geq 2$ kΩ; $V_O = \pm 10$ V	G_v	typ.	200 000	
Common mode rejection ratio	CMRR	typ.	90	dB
Differential input resistance	R_i	typ.	1	MΩ
Peak output voltage swing at $R_L = 10$ kΩ	V_{OM}	>	±12	V
Input voltage range	V_i	>	±12	V
Power dissipation	P_{tot}	typ.	50	mW

PACKAGE OUTLINE TO-99

Dimensions in mm



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

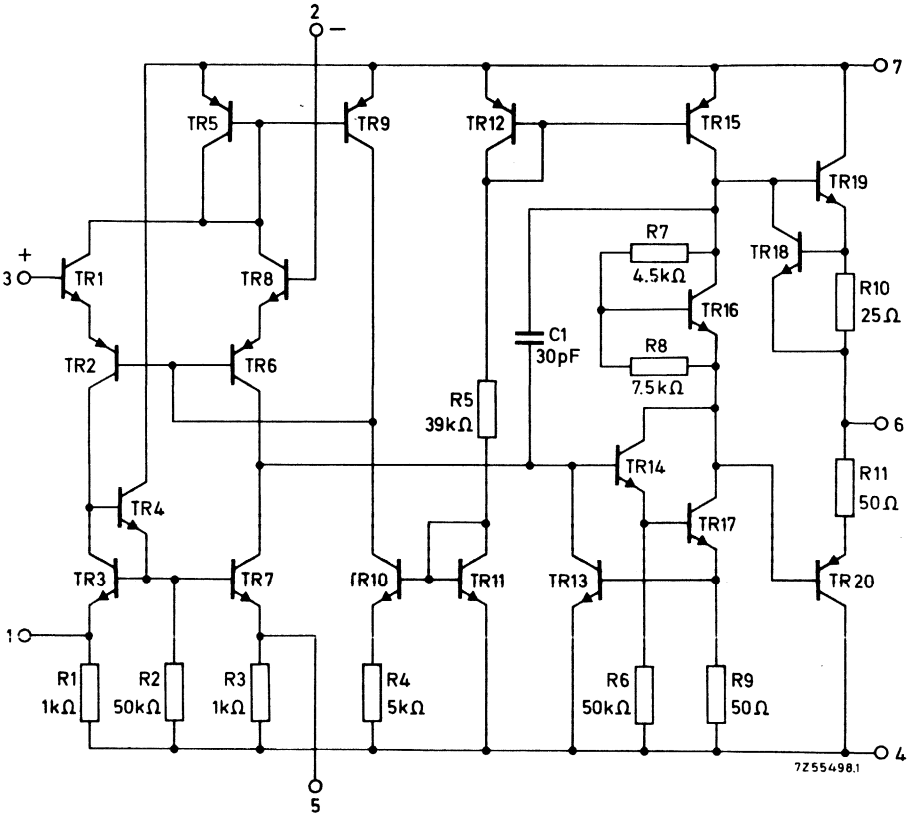
Voltages				
Positive supply voltage	V_P	max.	22	V
Negative supply voltage	$-V_N$	max.	22	V
Common mode input voltage [1]	V_i	max.	±15	V
Differential input voltage	V_{2-3}	max.	±30	V
Power dissipation [2]	P_{tot}	max.	500	mW
Output short circuit duration [3]		indefinite		
Temperatures				
Operating ambient temperature	T_{amb}	−55 to +125		°C
Storage temperature	T_{stg}	−65 to +150		°C

[1]) For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

[2]) Rating applies for case temperatures up to 125 °C; derate linearly at 6.5 mW/°C for ambient temperatures above 75 °C.

[3]) Continuous short circuit is allowed for case temperatures up to 125 °C and ambient temperatures up to 70 °C. Short circuit is allowed to ground or either supply.

CIRCUIT DIAGRAM

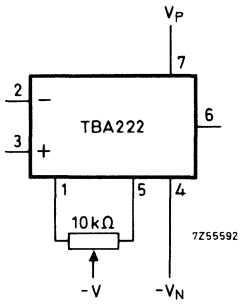


CHARACTERISTICS at V_P = 15 V; $-V_N$ = 15 V; T_{amb} = 25 °C unless otherwise specified

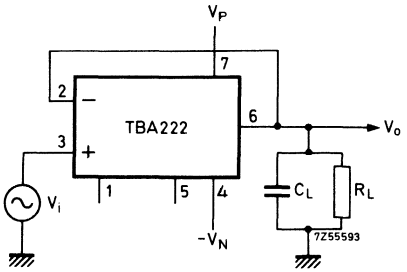
Voltage gain; $R_L \geq 2$ kΩ; V_O = ± 10 V	G_v	>	50 000	
		typ.	200 000	
Input offset voltage; $R_S \leq 10$ kΩ	V_{io}	typ.	1.0	mV
		<	5.0	mV
Input bias current	I_i	typ.	0.2	µA
		<	0.5	µA
Input offset current	I_{io}	typ.	30	nA
		<	0.2	µA
Common mode rejection ratio; $R_S \leq 10$ kΩ	CMRR	>	70	dB
		typ.	90	dB
Input voltage range	V_i	>	±12	V
		typ.	±13	V
Differential input resistance	R_i	>	0.3	MΩ
		typ.	1.0	MΩ
Supply voltage rejection ratio; $R_S \leq 10$ kΩ	SVRR	typ.	30	µV/V
		<	150	µV/V
Peak output voltage swing at $R_L \geq 10$ kΩ	V_{OM}	>	±12	V
		typ.	±14	V
$R_L \geq 2$ kΩ	V_{OM}	>	±10	V
		typ.	±13	V
Power dissipation at V_O = 0	P_{tot}	typ.	50	mW
		<	85	mW
Transient response (unity gain) V_i = 20 mV; R_L = 2 kΩ; $C_L \leq$ 100 pF				
Rise time		typ.	0.3	µs
Overshoot		typ.	5.0	%
Slew rate (unity gain) $R_L \geq 2$ kΩ		typ.	0.5	V/µs

CHARACTERISTICS at V_P = 15 V; $-V_N$ = 15 V; T_{amb} = −55 to +125 °C unless otherwise specified.

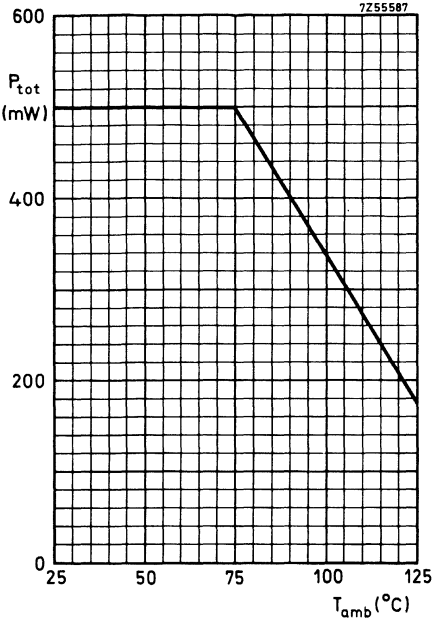
Voltage gain; $R_L \geq 2$ kΩ; V_O = ±10 V	G_v	>	25.000	
Input offset voltage; $R_S \leq 10$ kΩ	V_{io}	<	6	mV
Input bias current	I_i	<	1.5	μA
Input offset current	I_{io}	<	0.5	μA
Peak output voltage swing $R_L \geq 2$ kΩ	V_{OM}	>	±10	V

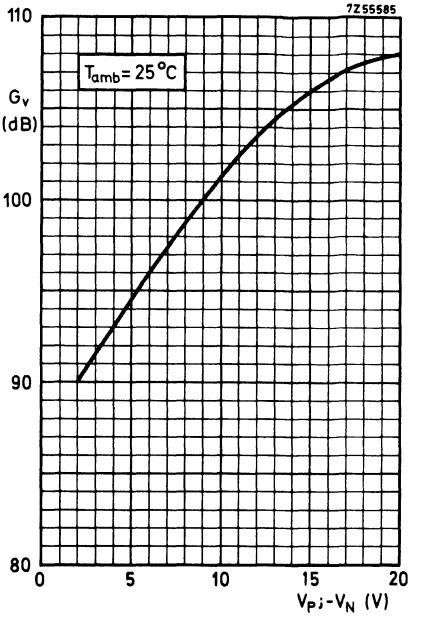


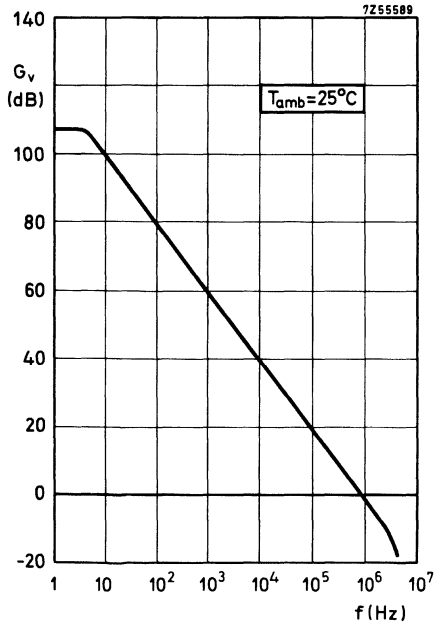
Offset voltage zeroing circuit

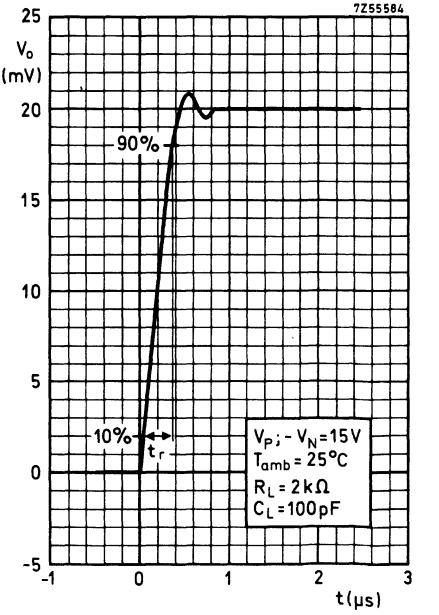


Transient response test circuit


7Z55587
600
400
200
0
P_{tot} (mW)
25
50
75
100
125
T_{amb} (°C)


7Z55585
110
100
90
80
G_v (dB)
T_{amb} = 25 °C
0
5
10
15
20
V_{Pi}-V_N (V)


7Z55589
140
100
80
60
40
20
0
-20
G_v (dB)
T_{amb}=25°C
1
10
10^2
10^3
10^4
10^5
10^6
10^7
f (Hz)

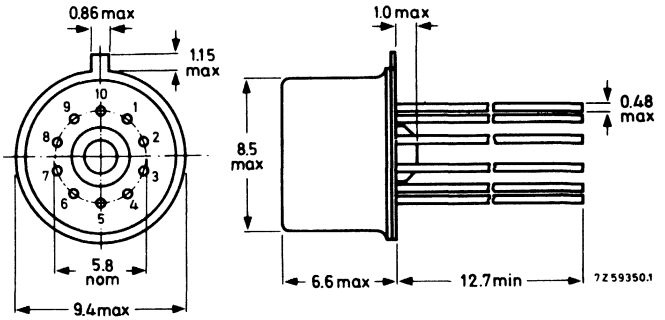

7Z55584
25
20
15
10
5
0
-5
V_o (mV)
90%
10%
t_r
V_{Pi} - V_N = 15 V
T_{amb} = 25 °C
R_L = 2 kΩ
C_L = 100 pF
-1
0
1
2
3
t (µs)

VOLTAGE REGULATOR

The TBA281 is a monolithic voltage regulator. It comprises a temperature compensated reference amplifier, an error amplifier, a power series pass transistor and current limit circuitry. External series pass transistors may be added if the load current exceeds the maximum limit. The circuit can be used with adjustable current limiting and remote shut down. It features low stand-by current drain, low temperature drift and high ripple rejection. The TBA281 can be used with positive or negative supply voltages as a series, shunt, switching or floating regulator in the ambient temperature range 0 to +70°C. The TBA281 is equivalent to the 723C.

QUICK REFERENCE DATA			
Line regulation V_i = 12V to 40V	typ.	0.1	$\%V_o$
Load regulation I_L = 1 mA to 50 mA	typ.	0.03	$\%V_o$
Stand-by current drain V_i = 30V, I_o = 0	typ.	2.3	mA
Input voltage range		9.5 to 40	V
Output voltage range		2.0 to 37	V
Input-output voltage difference		3.0 to 38	V

PACKAGE OUTLINE Dimensions in mm



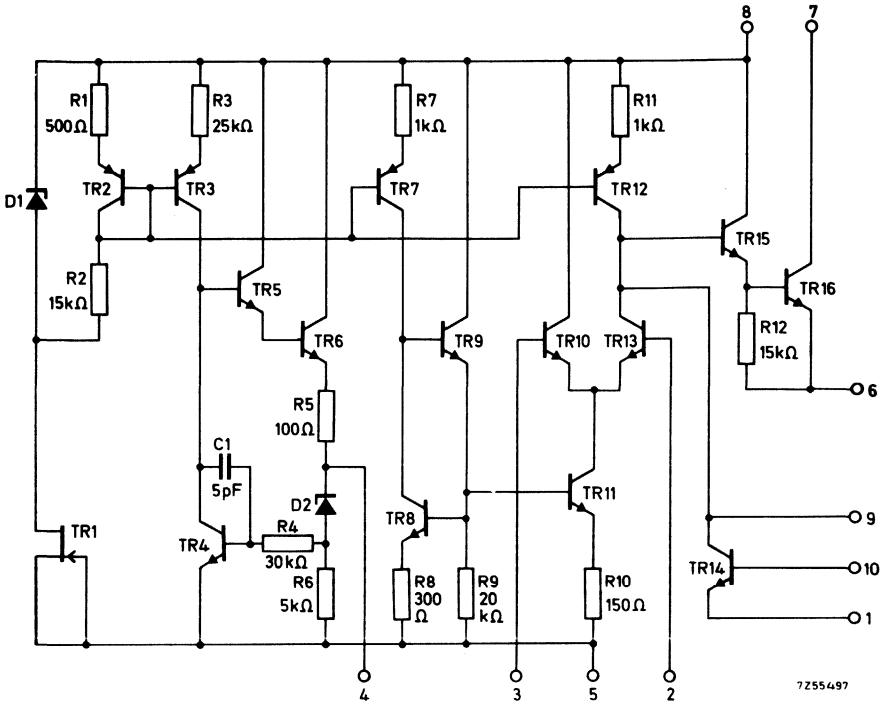
For details of pin numbering see page 3.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Input voltage	V_7	max.	40	V
Supply voltage	V_8	max.	40	V
Input-output voltage difference	V_{7-6}	max.	40	V
Currents				
Output current	$-I_6$	max.	150	mA
Current from reference amplifier output	$-I_4$	max.	15	mA
Power dissipation [1])	P_{tot}	max.	800	mW
Temperatures				
Operating ambient temperature	T_{amb}	0 to	+70	°C
Storage temperature	T_{stg}	−65 to	+150	°C

[1]) For operation above ambient temperature of 25 °C derate linearly at 6.8 mW/°C.

CIRCUIT DIAGRAM



PINNING

1. Current sense
2. Inverting input
3. Non-inverting input
4. **Reference voltage (V_{ref})**
5. Negative supply voltage ($-V_N$)
6. **Output voltage (V_o)**
7. **Collector voltage (V_C)**
8. Positive supply voltage (V_P)
9. Frequency compensation
10. Current limit

CHARACTERISTICS at $T_{amb} = 25\,^{o}C$; $V_i = V_P = V_C = 12V$; $-V_N = 0V$; $V_o = 5V$; $I_L = 5\,mA$, $R_{sc} = 0$; $C_1 = 100\,pF$; $C_{ref} = 0$ unless otherwise specified; (for testcircuit see figs. 1, 2 and 3 on page 5)

Line regulation				
at V_i = 12 to V_i = 15V		typ.	0.01	$\%V_o$
		<	0.1	$\%V_o$
at V_i = 12 to V_i = 40V		typ.	0.1	$\%V_o$
		<	0.5	$\%V_o$
at V_i = 12 to V_i = 15V; $T_{amb} = 0$ to $+70\,^{o}C$		<	0.3	$\%V_o$
Load regulation				
at I_L = 1 to I_L = 50 mA		typ.	0.03	$\%V_o$
		<	0.2	$\%V_o$
at I_L = 1 mA to I_L = 50 mA; $T_{amb} = 0$ to $+70\,^{o}C$		<	0.6	$\%V_o$
Ripple rejection at f = 50 Hz to 10 kHz				
$C_{ref} = 0$		typ.	74	dB
$C_{ref} = 5\,\mu F$		typ.	86	dB
Average temperature coefficient of output voltage at $T_{amb} = 0$ to $+70\,^{o}C$		typ.	0.003	$\%/^{o}C$
		<	0.015	$\%/^{o}C$
Short circuit current limit				
$R_{sc} = 10\Omega$; $V_o = 0$		typ.	65	mA
Reference voltage	V_4	typ.	7.15	V
			6.8 to 7.5	V
Output noise voltage at B = 100 Hz to 10 kHz				
$C_{ref} = 0$	V_n	typ.	20	μV
$C_{ref} = 5\,\mu F$	V_n	typ.	2.5	μV
Long term stability over 1000 hours			0.1	%
Stand-by current drain				
$I_L = 0$; $V_i = 30V$	I_P	typ.	2.3	mA
		<	4.0	mA
Input voltage range	V_i		9.5 to 40	V
Output voltage range	V_o		2.0 to 37	V
Input-output voltage difference	$V_i - V_o$		3.0 to 38	V

CHARACTERISTICS (continued)

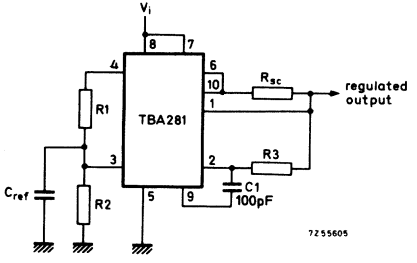


Fig. 1 [1][2]
Basic low voltage regulator
(V_O = 2 to 7V)
Typical performance
Regulated output voltage = 5V
Line regulation (ΔV_i = 3V) = 0.5mV
Load regulation (ΔI_L = 50mA) = 1.5mV

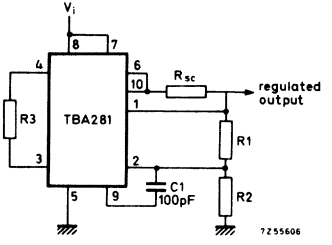


Fig. 2 [1][2]
Basic high voltage regulator
(V_O = 7 to 37V)
Typical performance
Regulated output voltage = 15V
Line regulation (ΔV_i = 3V) = 1.5mV
Load regulation (ΔI_L = 50mA) = 4.5mV

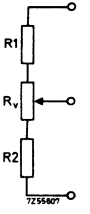


Fig. 3 [2]
Output voltage adjust

[1]) $R_3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum temperature drift. R_3 may be eliminated for minimum component count.

[2]) For adjustable output voltage replace R_1/R_2 in **fig. 1 and 2 with divider circuit** shown in fig. 3.

Formulae for intermediate output voltages

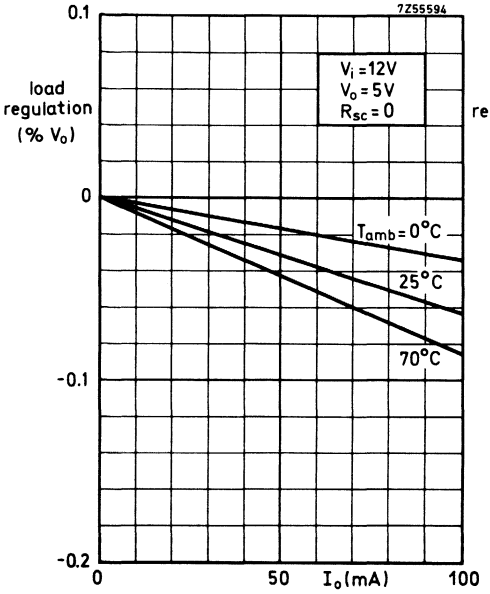
Outputs from +2 V to +7 V (fig. 1) $V_o = V_{ref} \times \frac{R_2}{R_1 + R_2}$

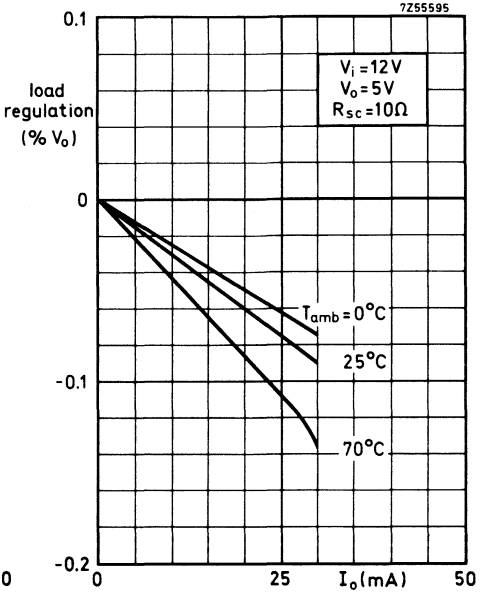
Outputs from +7 V to +37 V (fig. 2) $V_o = V_{ref} \times \frac{R_1 + R_2}{R_2}$

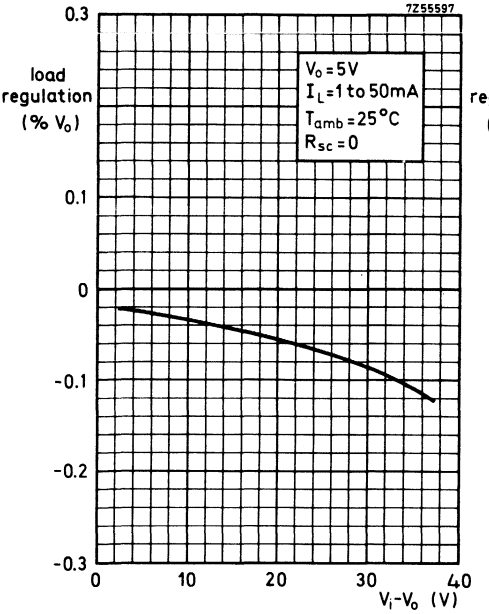
Resistor values (kΩ) for standard output voltages.

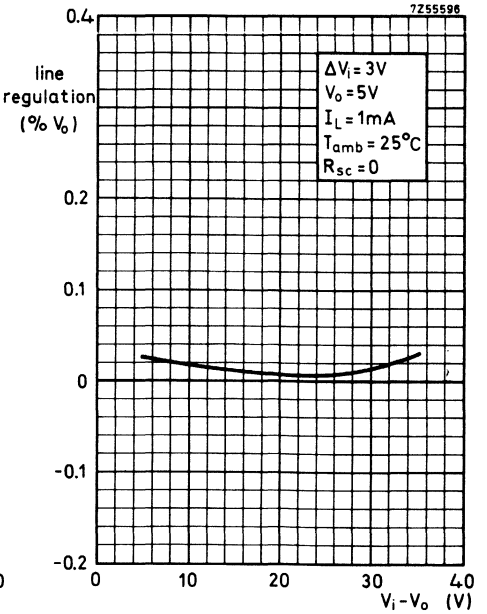
positive output voltage (V)	figure	fixed output ± 5%		adjustable output [1] ± 10% (see fig. 3)		
		R_1	R_2	R_1	R_v	R_2
+ 3.0	1	4.12	3.01	1.8	0.5	1.2
+ 3.6	1	3.57	3.65	1.5	0.5	1.5
+ 5.0	1	2.15	4.99	0.75	0.5	2.2
+ 6.0	1	1.15	6.04	0.5	0.5	2.7
+ 9.0	2	1.87	7.15	0.75	1.0	2.7
+ 12	2	4.87	7.15	2.0	1.0	3.0
+ 15	2	7.87	7.15	3.3	1.0	3.0
+ 28	2	21.0	7.15	5.6	1.0	2.0

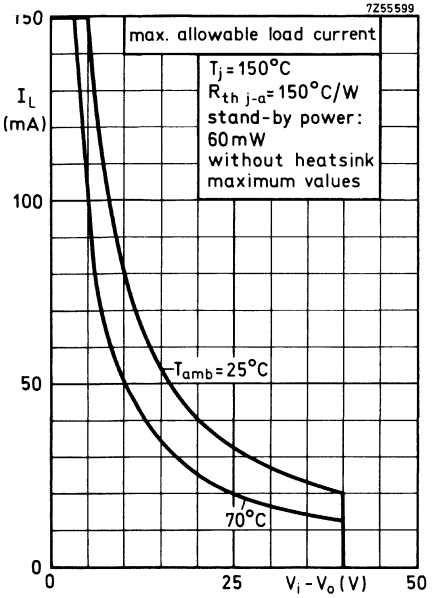
[1] For adjustable output voltage replace R_1/R_2 in fig. 1 and 2 with divider circuit shown in fig. 3 (on page 5).

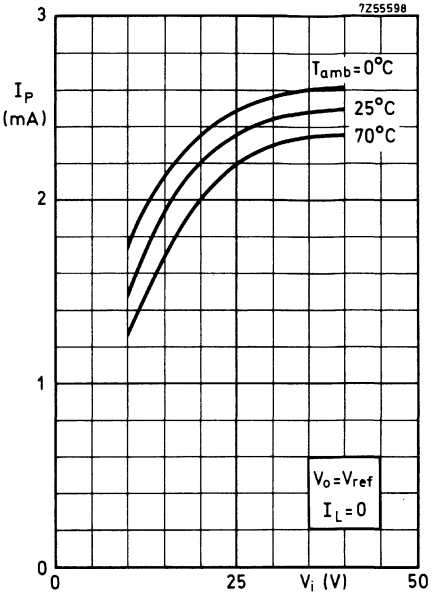

7Z55594
load regulation (% V_o)
V_i = 12V
V_o = 5V
R_{sc} = 0
T_{amb} = 0°C
25°C
70°C
0.1
0
-0.1
-0.2
0
50
100
I_o (mA)

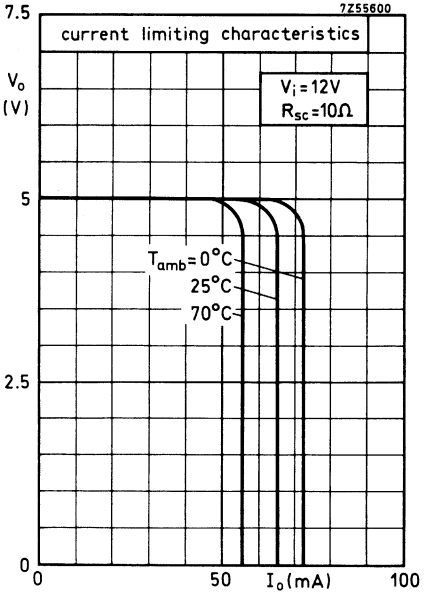

7Z55595
load regulation (% V_o)
V_i = 12V
V_o = 5V
R_{sc} = 10Ω
T_{amb} = 0°C
25°C
70°C
0.1
0
-0.1
-0.2
0
25
50
I_o (mA)

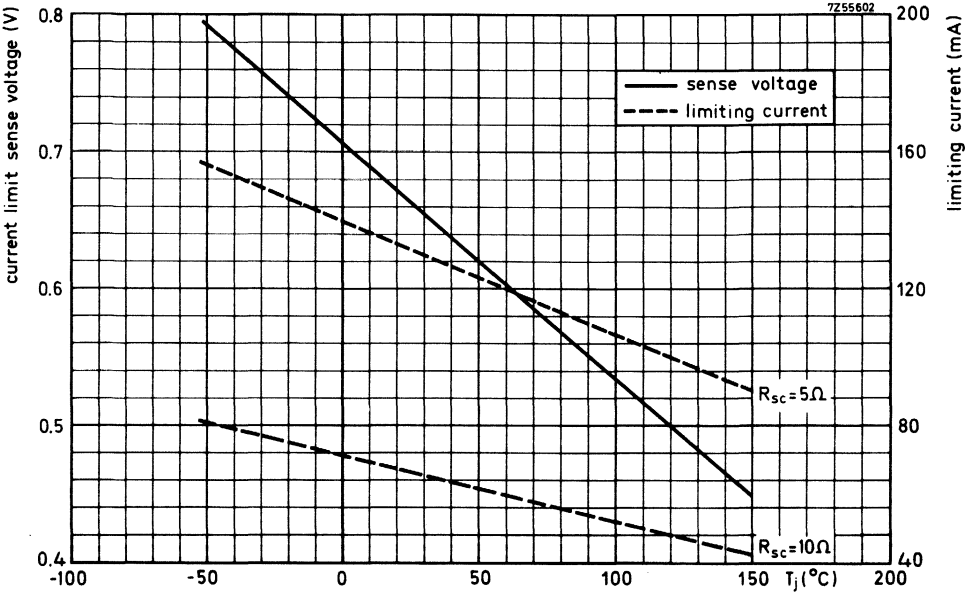

7Z55597
load regulation (% V_o)
V_o = 5V
I_L = 1 to 50mA
T_{amb} = 25°C
R_{sc} = 0
0.3
0.1
0
-0.1
-0.2
-0.3
0
10
20
30
40
V_i-V_o (V)

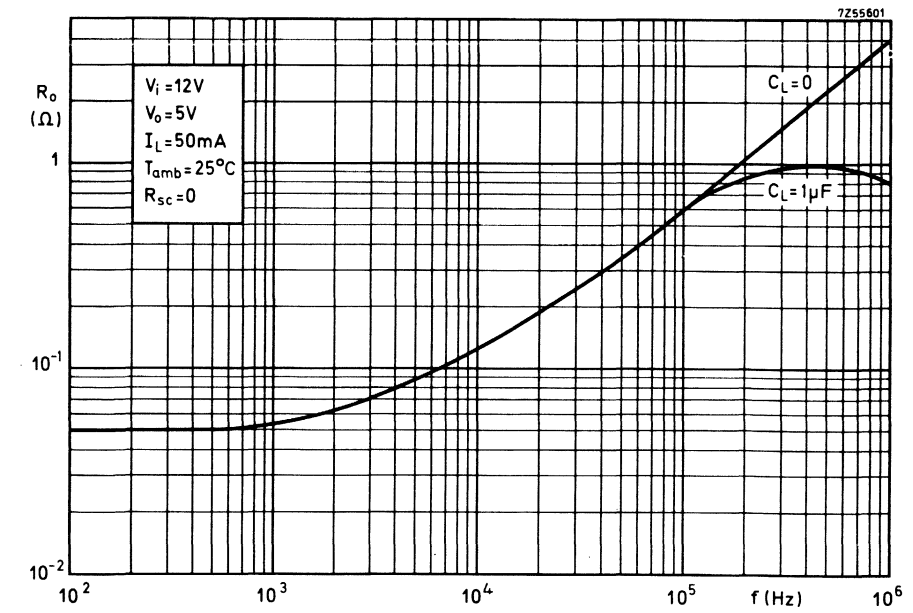

7Z55596
line regulation (% V_o)
ΔV_i = 3V
V_o = 5V
I_L = 1mA
T_{amb} = 25°C
R_{sc} = 0
0.4
0.2
0.1
0
-0.1
-0.2
0
10
20
30
40
V_i-V_o (V)

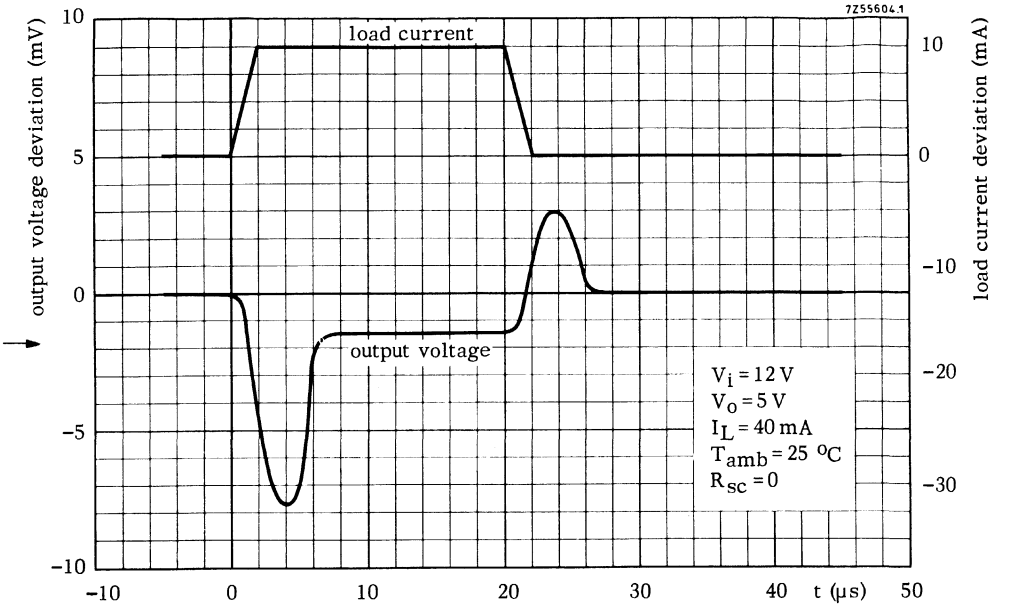

7Z55599
max. allowable load current
T_j = 150°C
$R_{th\ j\text{-}a}$ = 150°C/W
stand-by power:
60 mW
without heatsink
maximum values
I_L (mA)
150
100
50
0
T_{amb} = 25°C
70°C
0
25
$V_i - V_o$ (V)
50

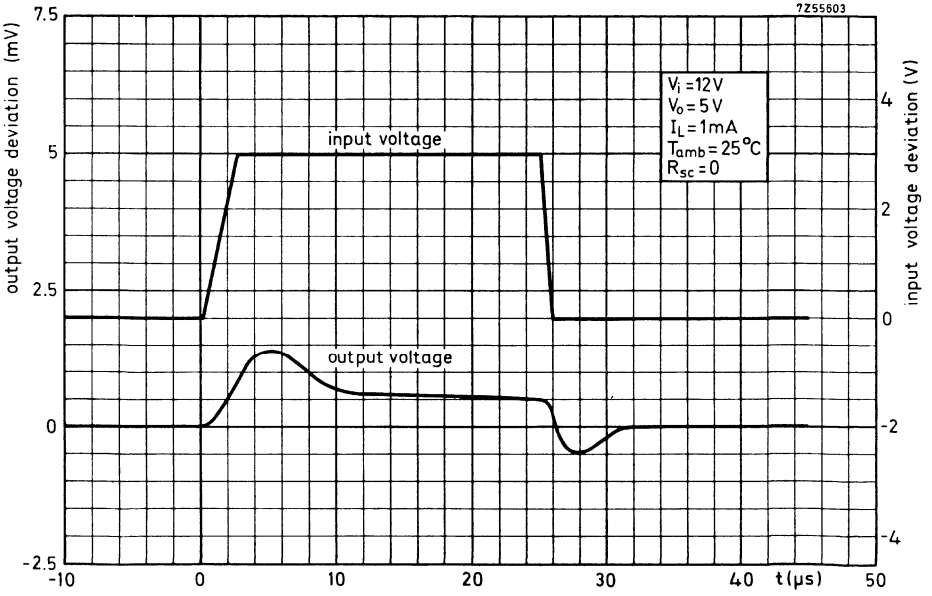

7Z55598
I_P (mA)
3
2
1
0
T_{amb} = 0°C
25°C
70°C
$V_o = V_{ref}$
I_L = 0
0
25
V_i (V)
50


7Z55600
current limiting characteristics
V_o (V)
7.5
5
2.5
0
V_i = 12V
R_{sc} = 10Ω
T_{amb} = 0°C
25°C
70°C
0
50
I_o (mA)
100


7Z55602
current limit sense voltage (V)
limiting current (mA)
sense voltage
limiting current
$R_{sc}=5\Omega$
$R_{sc}=10\Omega$
T_j(°C)
0.8
0.7
0.6
0.5
0.4
200
160
120
80
40
-100
-50
0
50
100
150
200


7Z55601
R_o (Ω)
V_i = 12V
V_o = 5V
I_L = 50mA
T_{amb} = 25°C
R_{sc} = 0
C_L = 0
C_L = 1μF
1
10^{-1}
10^{-2}
10^2
10^3
10^4
10^5
10^6
f (Hz)


7Z55604.1
load current
output voltage
output voltage deviation (mV)
load current deviation (mA)
10
5
0
-5
-10
-20
-30
-10
0
10
20
30
40
50
t (µs)
V_i = 12 V
V_o = 5 V
I_L = 40 mA
T_{amb} = 25 °C
R_{sc} = 0


7Z55603
input voltage
output voltage
output voltage deviation (mV)
input voltage deviation (V)
7.5
5
2.5
0
-2.5
4
2
0
-2
-4
-10
0
10
20
30
40
50
t(µs)
V_i = 12 V
V_o = 5 V
I_L = 1 mA
T_{amb} = 25 °C
R_{sc} = 0

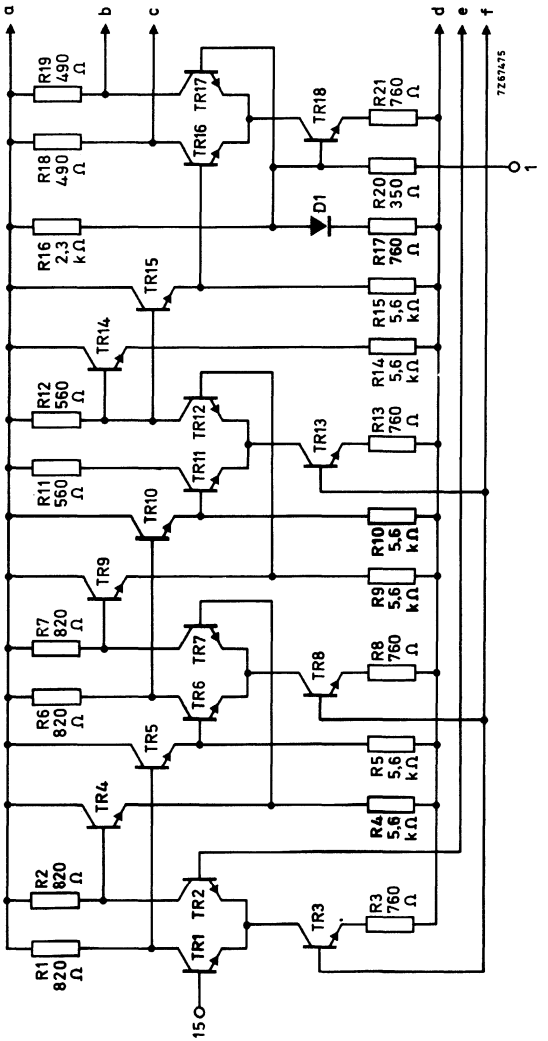
I.F. AMPLIFIER

The TBA480 is monolithic integrated four-stage i.f. amplifier with symmetrical f.m. detector, d.c. volume control and internally stabilized supply voltage.

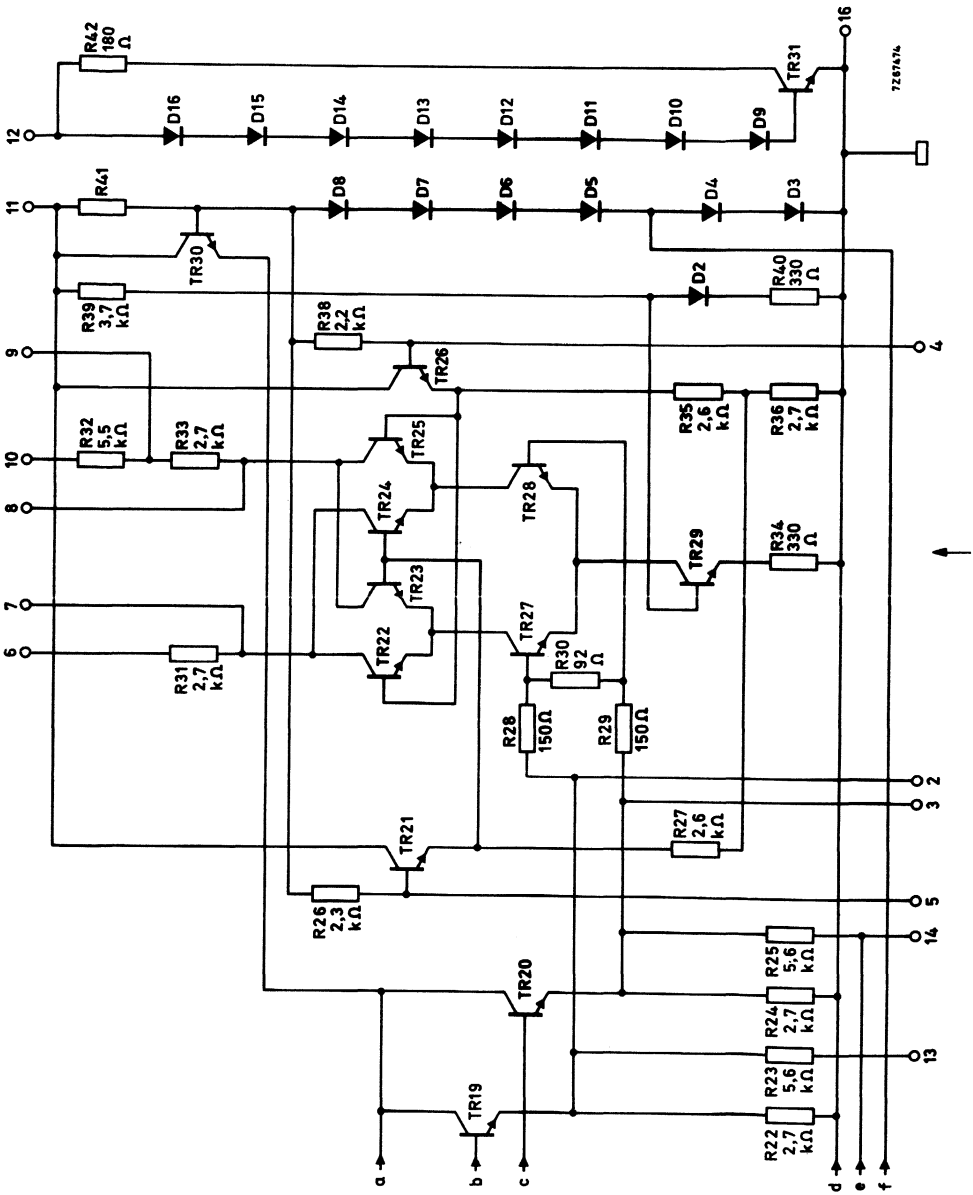
QUICK REFERENCE DATA				
Supply voltage	V_P	typ.	12	V
Ambient temperature	T_{amb}	typ.	25	^oC
Frequency	f_o		5,5	MHz
Input limiting voltage	V_{ilim}	typ.	55	μV
A.F. output voltage at $\Delta f = \pm 15$ kHz	$V_{o(rms)}$	typ.	320	mV
Control range of a.f. output	ΔV_o	≥	60	dB
A.M. rejection at $\Delta f = \pm 15$ kHz	α	≥	50	dB

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) (See General Section).

CIRCUIT DIAGRAM



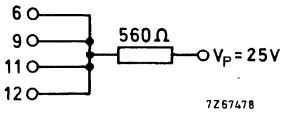
CIRCUIT DIAGRAM (continued)



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages					
→ Pin no. 11 voltage	V_{11-16}	max.	15	V	1)
→ Pin no. 6 voltage	V_{6-16}	max.	15	V	1)
→ Pin no. 9 voltage	V_{9-16}	max.	15	V	1)
Pin no. 10 voltage	V_{10-16}	max.	32	V	
→ Currents					
Total current	I_{tot}	max.	30	mA	2) 3)
Pin no. 12 current	I_{12}	max.	20	mA	4)
Total power dissipation	P_{tot}	max.	500	mW	5)
Temperatures					
→ Storage temperature	T_{stg}	−55 to +125		°C	
Operating ambient temperature	T_{amb}	−20 to +60		°C	

→ 1) 15 V may be exceeded if an external resistor of 560 Ω is used in accordance with diagram below.

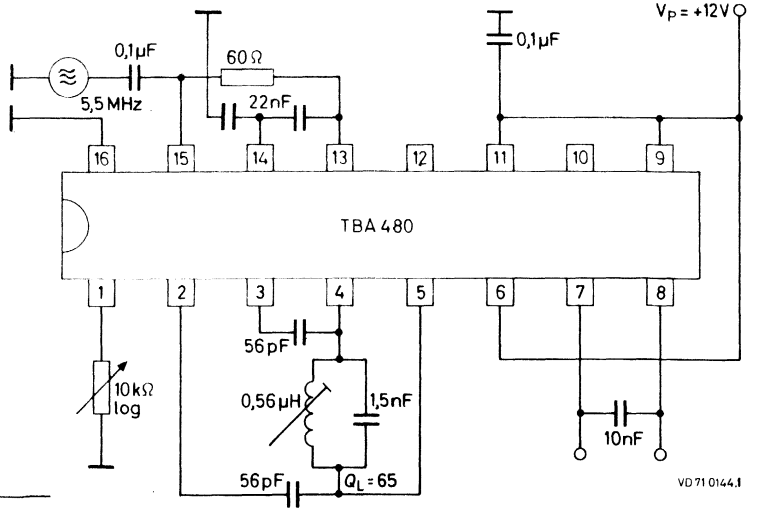


2) $I_{tot} = I_{11} + I_{12}$
3) Maximum 40 mA permissible while tubes are heating up.
→ 4) Maximum 25 mA permissible while tubes are heating up.
5) Maximum 640 mW permissible while tubes are heating up.

CHARACTERISTICS

For f.m.: i.f. amplifier at f_o = 5,5 MHz; V_P = 12 V; T_{amb} = 25 °C.

Voltages	V_{7-16} / V_{8-16}	typ.	8,5	V	[1]
Current	I_{11}	typ.	18	mA	
Input limiting voltage	$V_{i\,lim}$	typ. <	55 90	µV µV	
A.F. output voltage					
V_i = 5 mV; Δf = ± 15 kHz; f_m = 1 kHz	$V_{o(rms)}$	> typ.	240 320	mV mV	
Total distortion					
V_i = 5 mV; Δf = ± 50 kHz; f_m = 1 kHz	d_{tot}	typ. <	4,5 6	% %	
A.M. rejection					
for f.m.: Δf = ± 15 kHz; f_m = 70 Hz					
for a.m.: m = 0,3; f_m = 1 kHz					
at V_i = 300 µV	α	≥	45	dB	
at V_i = 1 mV	α	≥	50	dB	
at V_i = 100 mV	α	≥	50	dB	
Control output voltage range					
due to remote volume control	ΔV_o	≥	60	dB	

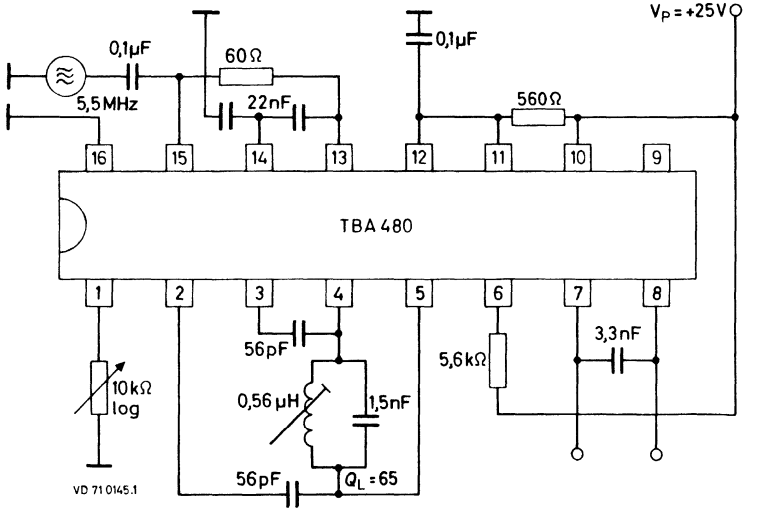


[1]) Difference V_{7-8} < ± 0,5 V

CHARACTERISTICS (continued)

For f.m.: i.f. amplifier at f_o = 5,5 MHz; V_P = 25 V; T_{amb} = 25 °C.

Voltages	V_{11-16} } V_{12-16} }		11 to 13	V	
	V_{7-16} } V_{8-16} }	typ.	13,5	V	
Total current	I_{tot}	typ. <	24 30	mA mA	1)
A.F. output voltage V_i = 5 mV; Δf = ± 15 kHz; f_m = 1 kHz	$V_{o(rms)}$	> typ.	700 950	mV mV	
Total distortion	} see page 5				
A.M. rejection	} see page 5				
Control output voltage range	} see page 5				

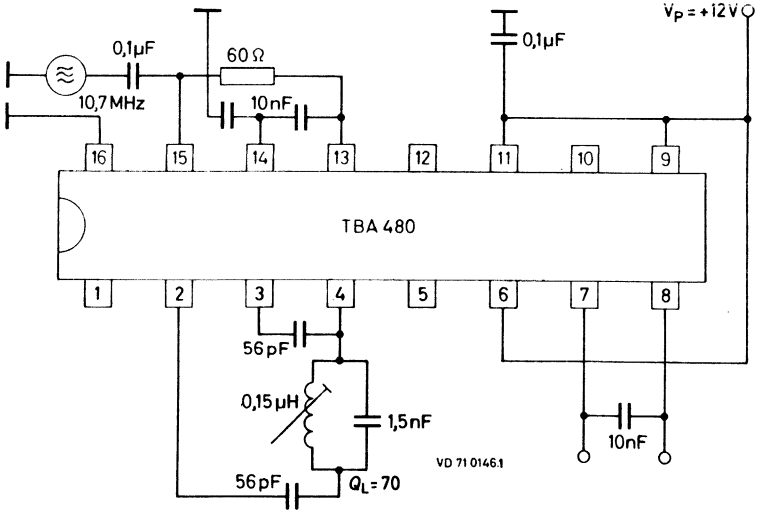


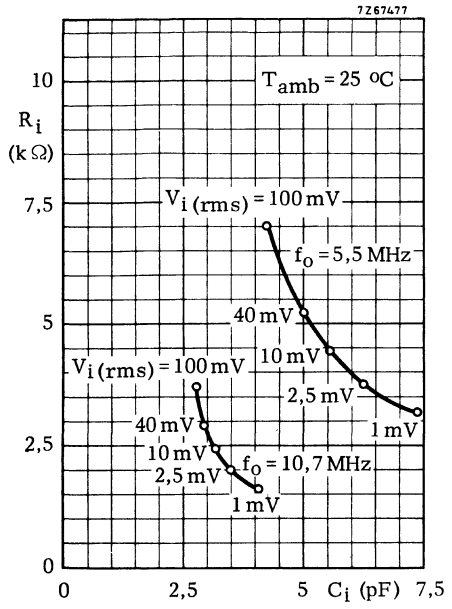
1) $I_{tot} = I_{11} + I_{12}$

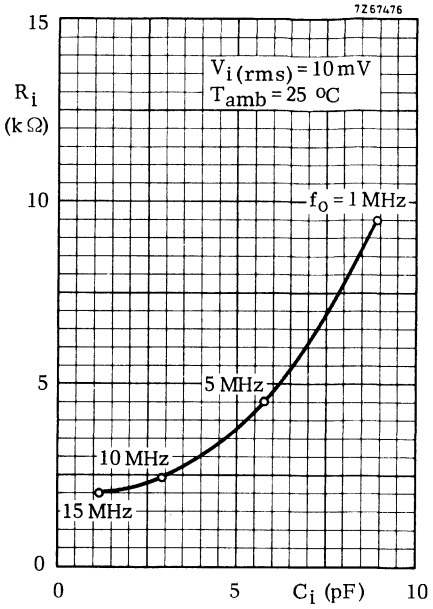
CHARACTERISTICS (continued)

For f.m.: i.f. amplifier at f_o = 10,7 MHz; V_P = 12 V; T_{amb} = 25 °C.

Current	I_{11}	typ. <	18 24	mA mA
Input limiting voltage	$V_{i\,lim}$	typ. <	75 120	μV μV
A.F. output voltage				
V_i = 5 mV; Δf = ± 15 kHz; f_m = 1 kHz	$V_{o(rms)}$	> typ.	130 180	mV mV
Total distortion				
V_i = 5 mV; Δf = ± 75 kHz; f_m = 1 kHz	d_{tot}	typ. <	4 5	% %
A.M. rejection				
for f.m.: Δf = ± 15 kHz; f_m = 50 Hz for a.m.: m = 0,3; f_m = 1 kHz				
at V_i = 300 μV	α	>	40	dB
at V_i = 1 mV	α	>	50	dB
at V_i = 100 mV	α	>	50	dB




7Z67477
10
7,5
5
2,5
0
R_i (kΩ)
T_{amb} = 25 °C
V_i (rms) = 100 mV
f_o = 5,5 MHz
40 mV
10 mV
2,5 mV
1 mV
V_i (rms) = 100 mV
40 mV
10 mV
2,5 mV
1 mV
f_o = 10,7 MHz
0
2,5
5
7,5
C_i (pF)


7Z67476
15
10
5
0
R_i (kΩ)
V_i (rms) = 10 mV
T_{amb} = 25 °C
f_o = 1 MHz
5 MHz
10 MHz
15 MHz
0
5
10
C_i (pF)

LUMINANCE COMBINATION

The TBA500N and TBA500P are integrated luminance amplifier circuits for colour television receivers incorporating delay line matching stages and a d.c. control which maintains a constant black level over its range of operation. A beam current limiting facility is provided, reducing the picture contrast first and then brightness.

The TBA500N is intended to be used if the voltage for beam current limiting is negative going whereas the TBA500P should be used if this voltage is positive going.

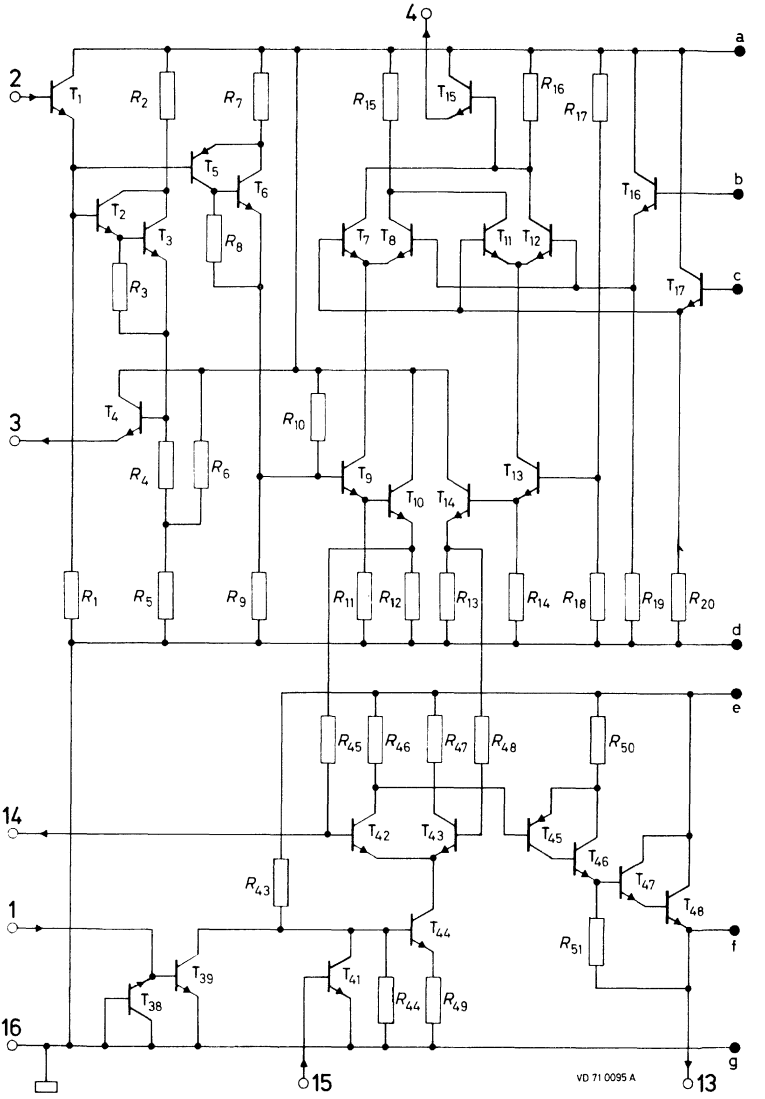
Horizontal and vertical blanking pulses may be applied.
An a.g.c. detector is incorporated for tuner (p-n-p) and if amplifier (n-p-n); this circuit can, however, also be used as a gated luminance black level clamp.

QUICK REFERENCE DATA				
Supply voltage	V_{12-16}	nom.	12	V
Input signal (peak-to-peak value)	$V_{2-16(p-p)}$	typ.	2	V
Output signal (peak-to-peak value)	$V_{10-16(p-p)}$	typ.	4	V
Linearity at maximum contrast	m	>	0,9	

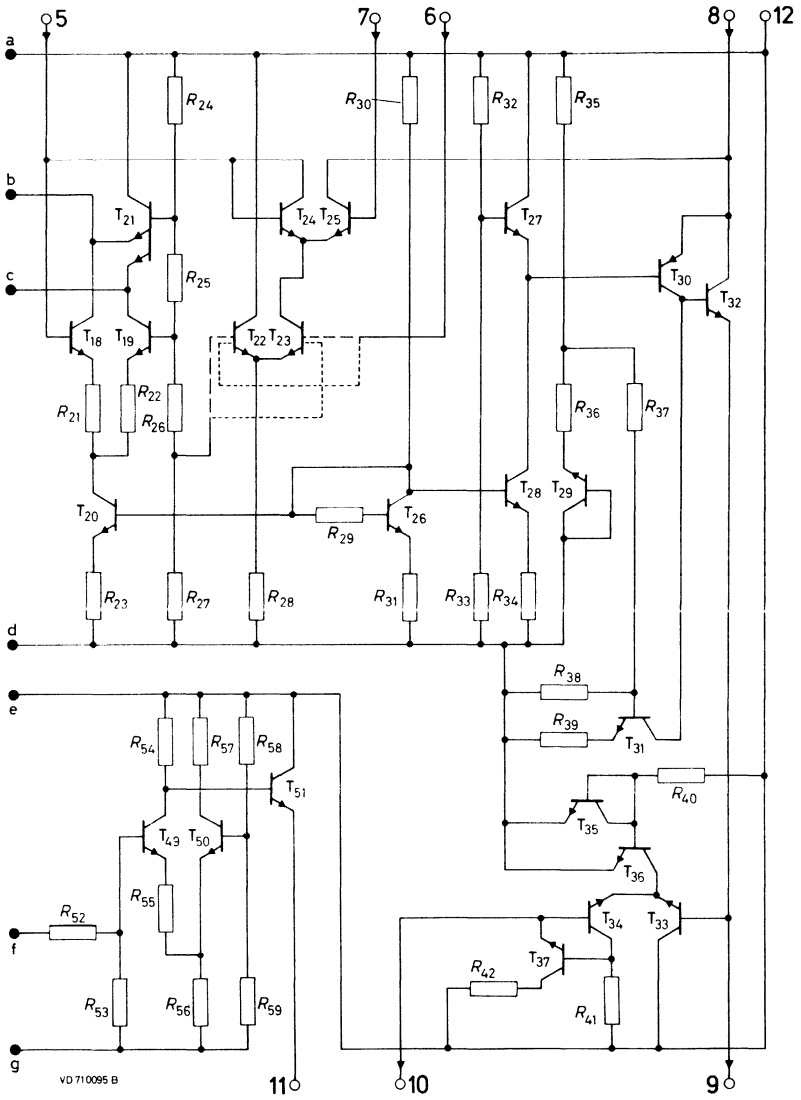
PACKAGE OUTLINE

TBA500N and TBA500P : 16 lead plastic dual in-line (type A) (See General Section)
TBA500NQ and TBA500PQ: 16 lead plastic quadruple in-line (See General Section)

CIRCUIT DIAGRAM



CIRCUIT DIAGRAM (continued)



Note

Pin 6 connection to transistors T22 or T23
TBA500N: connections made via dotted lines (------)
TBA500P: connections made via dashed lines (– – – –)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage				
Supply voltage	V_{12-16}	max.	13,2	V
Current				
Peak current in pin 13	I_{13M}	max.	400	mA [1])
Current at pin 1	$+I_1$	max.	5	mA
	$-I_1$	max.	10	mA
Current at pin 15	$+I_{15}$	max.	15	mA
	$-I_{15}$	max.	1	mA
Power dissipation				
Total power dissipation	P_{tot}	max.	600	mW
Temperatures				
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		−20 to + 60	°C

[1]) At pulse duration $t_p \leq 1$ µs; repetition frequency 16 kHz.

CHARACTERISTICS at V_{12-16} = 12 V: T_{amb} = 25 °C; See circuit on page 7.

Luminance input (negative going sync with respect to positive supply)

Input signal (peak-to-peak value)	$V_{2-16(p-p)}$	typ.	2	V
Input impedance	$\|Z_{2-16}\|$	≥	50	kΩ

Luminance output

Output signal (peak-to-peak value)	$V_{10-16(p-p)}$	typ.	4	V
Output voltage range	V_{10-16}	0,2 to	4,5	V
Output impedance	emitter follower output			
3 dB bandwidth without delay line	B	>	5	MHz
Contrast control range		>	36	dB
Contrast adjustment voltage range	V_{5-16}	1,5 to	4,5	V
Linearity at maximum contrast	m	>	0,9	
Brightness control range	ΔV_{10-16}	typ.	1,3	V

Video signal for sync separator and chrominance amplifier

(with positive going sync)

Output signal (peak-to-peak value)	$V_{3-16(p-p)}$	typ.	3	V
Output impedance	emitter follower output			
3 dB bandwidth	B	>	5	MHz

Delay line

Delay lines with characteristic impedances in the range 1 kΩ to 2,7 kΩ can be used with external matching resistors. No capacitive load on delay line.
The frequency response and magnitude of maximum output signal can be adjusted by means of external components (pin 9).

Blanking

For horizontal and vertical blanking apply a negative pulse current into pin 8.

Beam current limiting

Voltage for start of limiting	V_{6-16}	typ.	2	V [1]

[1]) Voltage negative going for TBA500N
Voltage positive going for TBA500P

CHARACTERISTICS (continued)

A.G.C. detector

A.G.C. voltage for i.f. amplifier	V_{13-16}	0	to 9	V
A.G.C. voltage for tuner	V_{11-16}	11	to 3	V
A.G.C. take-over point	V_{13-16}	typ.	6,5	V
I.F. amplifier control voltage variation over tuner control voltage range	ΔV_{13-16}	typ.	2	V

Gating pulses for a.g.c. [1])

a.g.c. is active only if: $V_{1-16} < 0,3$ V and $V_{15-16} < 0,3$ V

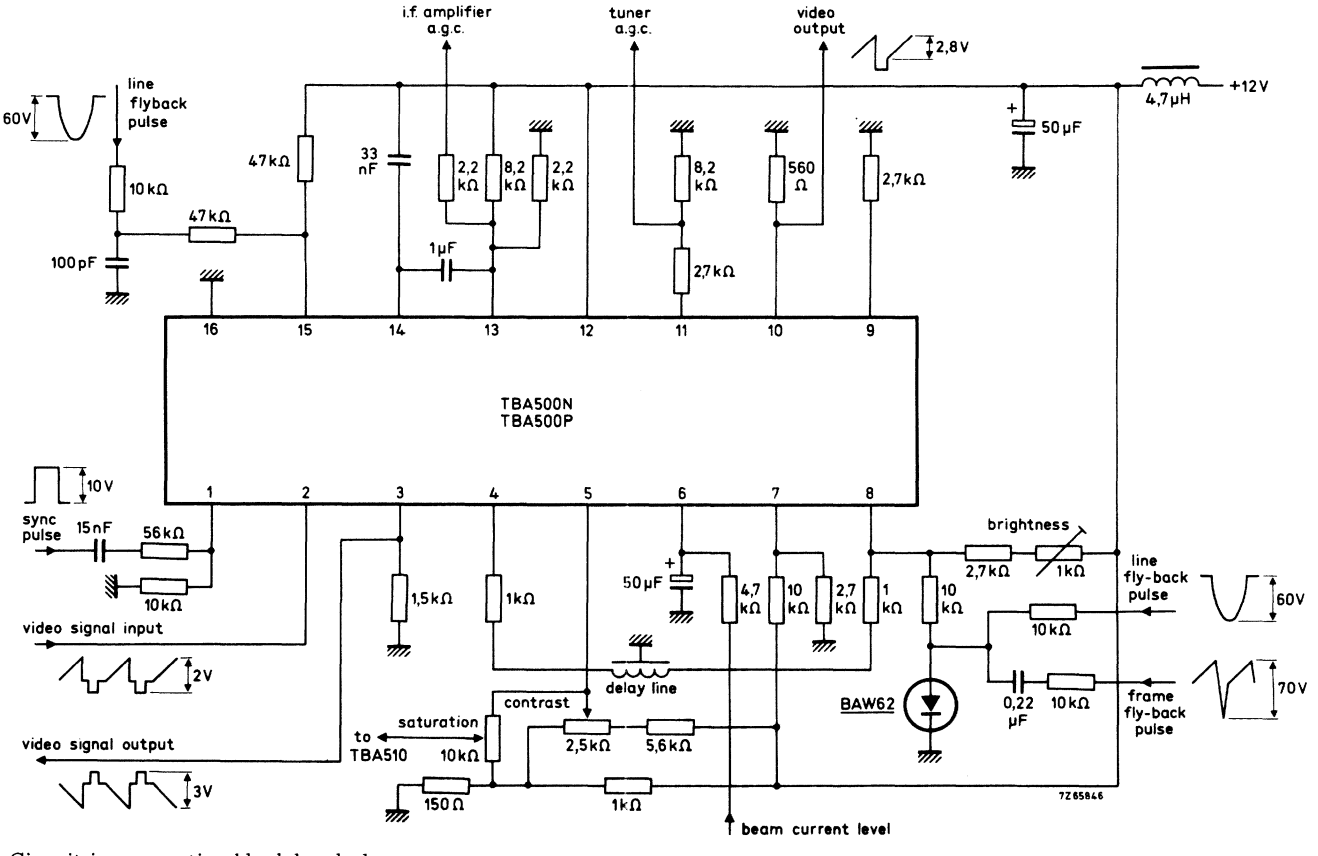
a.g.c. is not active if :
a. $I_1 > 0,1$ mA ($V_{1-16} \approx 0,7$ V) and $V_{15-16} < 0,3$ V
b. $V_{1-16} < 0,3$ V and $I_{15} > 0,1$ mA ($V_{15-16} \approx 0,7$ V)
c. $I_1 > 0,1$ mA ($V_{1-16} \approx 0,7$ V) and $I_{15} > 0,1$ mA ($V_{15-16} \approx 0,7$ V).

PINNING

1. Sync input
2. Video signal input
3. Video signal output
4. Luminance delay line drive output
5. D.C. contrast control input
6. Beam current limiting input
7. Beam current threshold
8. Input for output signal of luminance delay line.
9. Luminance compensation
10. Luminance signal output
11. Tuner a.g.c.
12. Supply voltage (12 V)
13. Black level clamp output or i.f. - a.g.c.
14. Filtering
15. Black porch key pulse input
16. Earth (negative supply)

[1]) The inputs for gating pulses (pins 1 and 16) are provided with NOR-gates.

APPLICATION INFORMATION



Circuit incorporating black level clamp.

APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number.

1. Positive-going sync waveform input for sync-cancelling the black level clamp

   Any convenient source of separated sync waveform may be employed.

2. Video signal input

   A signal of 2 V peak-to-peak amplitude with negative going sync pulses is required. The black level of the signal has to be +10, 4 V.

3. Video signal output

   A composite video signal of 3 V peak-to-peak amplitude and having a positive-going sync pulses is produced from an internal emitter follower. This can be used as a source of chroma signal or as a source of sync pulses if required.

4. Delay line driver output

   A low impedance signal source to feed the delay line input terminating resistor. Luminance delay lines having characteristic impedances in the range 1 kΩ to 2, 7 kΩ can be used. The signal at pin 4 is controlled by the contrast control and beam current limiting function.

5. D.C. contrast control potential

   A control range of 36 dB at least can be achieved by a variation of 1, 5 to 4, 5 V on pin 5. There is a linear relationship between the video signal amplitude on pin 4 and the potential on pin 5.

6. Beam current limiting input

   A rising positive potential on pin 6 of the TBA500N will start to reduce the picture contrast at about +2 V. A further increase in potential on pin 6 will continue to reduce the contrast until a threshold is reached (determined by the potential applied to pin 7) where the video signal d.c. level will be reduced giving a reduction in picture brightness.
   The same procedure holds for the TBA500P if the potential at pin 6 is negative going.

7. Beam current limiting threshold potential (brightness reduction threshold only).

8. Input for luminance delay line output

   This pin has a d.c. potential of about 6, 6 V and acts as a "current sink". The current fed into pin 8 comes out again at pin 9 after an impedance transformation. Brightness control and horizontal and vertical flyback blanking pulses are also applied to pin 8.

9. Load resistor for the luminance amplifier

   The network to pin 9 determines the gain of the luminance amplifier and its frequency response.

APPLICATION INFORMATION (continued)

10. Luminance signal output

An internal emitter follower provides the output signal across an external load resistor. The available output voltage range is from +0, 2 to +4, 5 V. The potential of the black level of the output signal would normally be set to +1, 5 V by appropriate setting of the current into pin 8. A luminance signal output amplitude of 4 V peak-to-peak at maximum contrast is produced. Superimposed on the latter is the blanking waveform which will remain of constant amplitude independently of contrast and brightness adjustments.

11. Control voltage for tuner

12. Positive 12 V supply

13. Output of black level keyed a.g.c. detector

14. Low pass filter capacitor

This filter prevents the operation of the black level clamp being affected by the colour burst or h.f. noise.

15. Back porch key pulse input

This can be produced from the line timebase flyback pulse by either a differentiating (short flyback time) or ringing coil (long flyback time) network. A margin of overlap with the line sync pulse on the video waveform is tolerable because of the use of sync cancelling in the clamp circuit. However, the clamp pulse should not be permitted to encroach uppon the following picture line.

16. Negative supply (earth)

CHROMINANCE COMBINATION

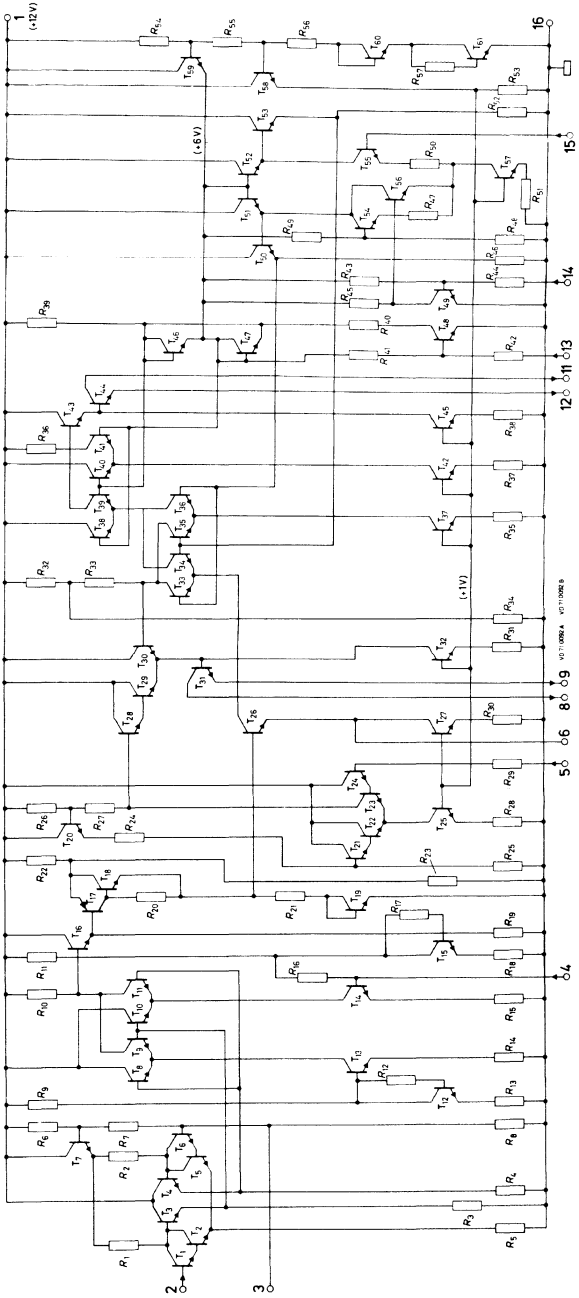
The TBA510 is an integrated chrominance amplifier circuit for colour television receivers incorporating a variable gain a.c.c. chroma amplifer circuit, a d.c. control for chroma saturation which can be ganged to the receiver contrast control, chroma blanking and burst gating functions, a burst output stage, a colour killer stage and a P.A.L. delay line driver stage.

QUICK REFERENCE DATA				
Supply voltage	V_{1-16}	nom.	12	V
Input signal (colour bars) peak-to-peak value	$V_{4-16(p-p)}$	nom.	150	mV
Output signal (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	1	V
Burst signal output (peak-to-peak value)	$V_{12-16(p-p)}$	typ.	1	V

PACKAGE OUTLINE:

TBA510 : 16 lead plastic dual in-line (type A) (See General Section).
TBA510Q: 16 lead plastic quadruple in-line (See General Section).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage				
Supply voltage	V_{1-16}	max.	13.2	V
Currents	I_8 ; I_{11}	max.	20	mA
	$-I_9$; $-I_{12}$	max.	20	mA
Power dissipation				
Total power dissipation	P_{tot}	max.	550	mW
Temperatures				
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		−20 to +60	°C

CHARACTERISTICS at V_{1-16} = 12 V; T_{amb} = 25 °C ; See also test circuit on page 5.

Input of chrominance signal (fed in via 1 nF)				
Input voltage (peak-to-peak value)	$V_{4-16(p-p)}$	typ.	150	mV
Input voltage range	V_{4-16}		15 to 300	mV
Input impedance	$\|Z_{4-16}\|$	>	2	kΩ
		typ.	3	kΩ
Output of burst signal				
D.C. voltage	V_{12-16}	typ.	8	V
Output signal (peak-to-peak value)	$V_{12-16(p-p)}$	typ.	1	V[1])
Collector current of output transistor TR44	I_{11}	typ.	4	mA
Chrominance signal output (without burst)				
D.C. voltage	V_{9-16}	typ.	7	V
Output signal (colour bars) at nominal saturation and maximum contrast (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	1	V
Range of contrast and saturation control			+6 to −30	dB
Collector current of output transistor TR31	I_8	typ.	5	mA
Input of a.c.c.				
A.C.C. voltage for maximum gain	V_{2-16}	typ.	2.5	V
Input impedance	Z_{2-16}	>	50	kΩ

1) Kept constant by a.c.c. circuit

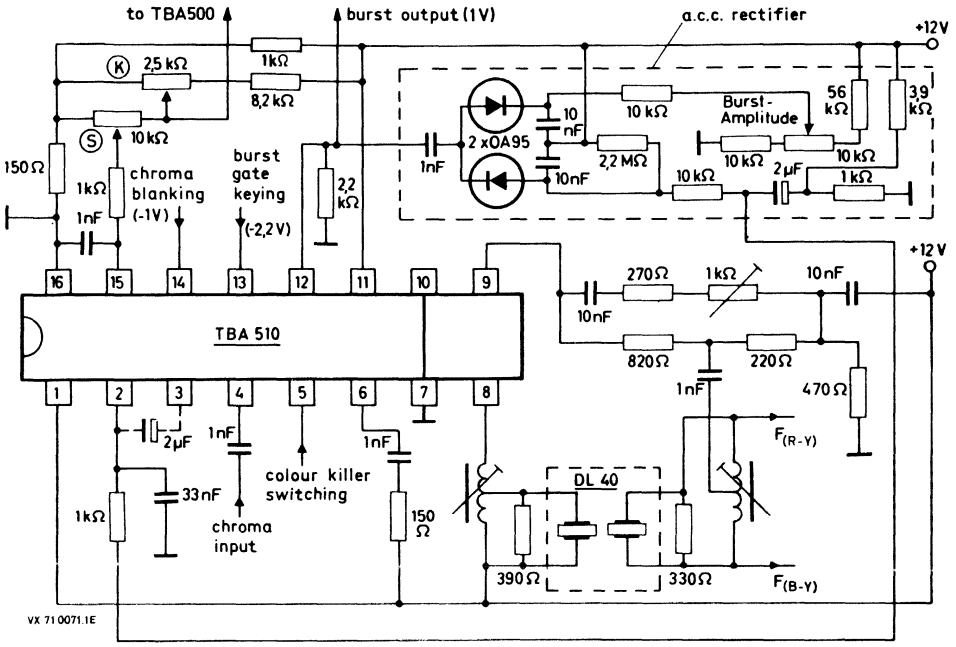
CHARACTERISTICS (continued)

Input of chroma-saturation control				
Control voltage range	V_{15-16}		1.5 to 4.5	V
Input impedance	$\lvert Z_{15-16} \rvert$	>	50	kΩ
Input of chroma blanking				
Switching level range	$-V_{14-16}$		1 to 5	V
Input impedance	$\lvert Z_{14-16} \rvert$	typ.	2	kΩ
Input of burst gate				
Switching level range	$-V_{13-16}$		2.2 to 5.0	V
Input impedance	$\lvert Z_{13-16} \rvert$	typ.	4	kΩ
Input of colour killer				
Input voltage for: colour on	V_{5-16}		2.5 to 4	V
for: colour off	V_{5-16}		0 to 1.8	V
Signal suppression at colour off		>	50	dB
Input impedance	$\lvert Z_{5-16} \rvert$	>	150	kΩ

PINNING

1. Supply voltage (12 V)
2. A.C.C. control potential input
3. A.C.C. bias ripple compensation
4. Chroma signal input
5. Colour killer switching input
6. Emitter decoupling network
7. Screen
8. Chroma delay line driver (collector)
9. Chroma delay line driver (emitter)
10. Screen
11. Colour burst output (collector)
12. Colour burst output (emitter)
13. Burst gate gating pulse
14. Chroma blanking pulse input
15. Chroma saturation control
16. Earth (negative supply)

APPLICATION INFORMATION



The function is quoted against the corresponding pin number

1. Positive 12V supply
2. A.C.C. control potential input
   The potential required at pin 2 for maximum gain is about 2,5 V; gain reduction occurs when this potential is reduced, $Z_{in} > 50$ kΩ
3. A.C.C. bias ripple compensation
   The internal A.C.C. circuit consists of a longtailed pair system. The "cold" side is established internally at +2.5 V and is brought out on pin 3. This enables a decoupling capacitor to be connected and returned to the point which secures the lowest supply line ripple amplitude injection into the a.c.c. loop.
4. Chroma signal input
   The allowable input voltage range is from 15 mV to 300 mV peak-to-peak with a colour bar signal. The input impedance is greater than 2 kΩ.

APPLICATION INFORMATION (continued)

5. Colour killer switching input
The input impedance is greater than 50 kΩ. Colour "on" 2.5 to 4 V; colour "off" 0 to 1.8 V. The chroma signal suppression when killed is greater than 50 dB.

6. Emitter decoupling network
The series network decouples an emitter of an amplifier stage in the chroma channel. The value of resistance influences the chroma channel gain.

7. Screen
This pin must be connected to pin 10 and taken via a direct path to earth. The function of this is to prevent burst and unwanted chroma appearing at the chroma output of the integrated circuit.

8. Delay line driver (collector)
Supplies the chroma signal drive to the delay line driver transformer, the cold end of which is connected to +12 V. The maximum permitted voltage excursion at this pin is 20 V peak. Maximum current, 12 mA peak.

9. Delay line driver (emitter)
Supplies the chroma to the network which provides the non-delayed signal to the delay line output transformer. The emitter is established internally at a potential of 6.8 ± 1V and the external network, which must incorporate a resistive d.c. path to earth, must not demand more than 20 mA peak current.

10. Screen
Connect to pin 7 and then to earth.

11. Colour burst output (collector)
If a low impedance colour burst is required (from the emitter of the colour burst output, pin 12) pin 11 will be connected to the +12 V supply. The maximum voltage and current excursions permitted on pin 11 are 20 V peak and 20 mA peak.

12. Colour burst output (emitter)
An external load resistor of 2 kΩ is required connected to earth and d.c. potential of 7.7 ± 1V is established on pin 12 due to the internal circuitry. The burst output voltage is 1 V peak-to-peak.

13. Burst gate gating pulse
The horizontal flyback pulse can be used as a source of gating waveform. A negative-going pulse of not greater than 5 V amplitude is necessary, the input impedance is 4 kΩ and the switching level is between −2.2 V and −5 V.

14. Chroma blanking pulse input
A negative going horizontal flyback pulse can be used here. Its amplitude should not exceed −5 V. The input impedance at this pin is 2 kΩ and the switching level is about −1.0 V.
During scan time, the d.c. voltage on this pin should not be negative.

APPLICATION INFORMATION (continued)

15. Chroma saturation control
The d.c. control voltage range required is from 1.5 to 4.5 V (highest gain at 4.5 V).
The input impedance is > 50 kΩ and a control range from +6 to -30 dB is given.

16. Negative supply or earth

COLOUR DEMODULATOR

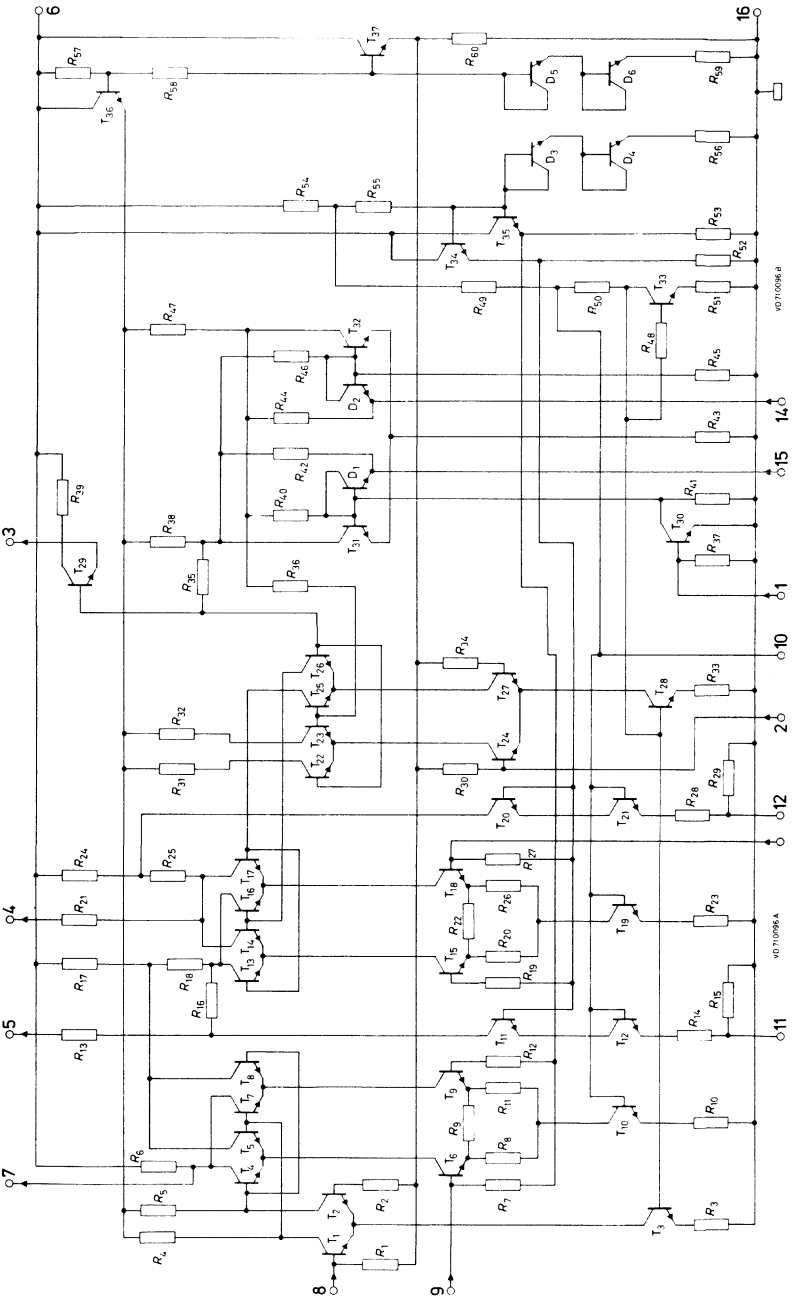
The TBA520 is an integrated colour demodulator circuit for colour television receivers, incorporating two active synchronous demodulators for R-Y and B-Y chrominance signals, a matrix (producing the G-Y colour difference signal), P.A.L. phase switch and flip-flop. It is suitable for d.c. -coupled drive to the picture tube when associated with the matrix integrated circuit (TBA530) and R.G.B. output stages.

QUICK REFERENCE DATA				
Supply voltage (stabilised)	V_{6-16}	nom.	12	V
Ambient temperature	T_{amb}		25	^{o}C
Gain of R-Y demodulator	G_{13-4}	typ.	7	
Gain of B-Y demodulator	G_{9-7}	typ.	12.5	
Impedance of chrominance inputs	$\|Z_{9-16}\|$ $\|Z_{13-16}\|$	typ.	1 kΩ in parallel with 10 pF	
Impedance of colour-difference signal outputs	$\|Z_{4-16}\|$	typ.	2.7	kΩ
	$\|Z_{7-16}\|$	typ.	2.7	kΩ
	$\|Z_{5-16}\|$	typ.	2.7	kΩ

PACKAGE OUTLINE :

TBA520 : 16 lead plastic dual in-line (type A) (See General Section).
TBA520Q: 16 lead plastic quadruple in-line (See General Section).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134).

Voltages				
Supply voltage	V_{6-16}	max.	13.2	V
Ident voltage	$-V_{1-16}$	max.	5	V
Current				
Ident current	I_1	max.	1	mA
Power dissipation				
Total power dissipation	P_{tot}	max.	550	mW
Temperatures				
Storage temperature	T_{stg}	−55 to +125		°C
Operating ambient temperature	T_{amb}	−20 to + 60		°C

CHARACTERISTICS at V_{6-16} = 12 V (stabilised); T_{amb} = 25 °C

Gain of chrominance (R-Y) signal				
$V_{i(p-p)}$ = 50 mV; f = 4.4 MHz	G_{13-4}	typ.	7	1)
Ratio of gain of blue channel to red channel at identical input signal voltages	$\frac{G_{9-7}}{G_{13-4}}$	typ.	1.78	
Matrix for generation G-Y signal	−0.51 (R-Y) −0.19 (B-Y)			
Colour-difference d.c. output voltages	V_{4-16}	typ.	7.9	V
	V_{7-16}	typ.	7.9	V
	V_{5-16}	typ.	7.9	V
Drift d.c. output voltage ΔT_{amb} = 40 °C		≤	50	mV
Relative change of d.c. output voltages between channels at ΔT_{amb} = 40°C		≤	20	mV
Colour difference output signals peak to peak values R-Y	$V_{4-16(p-p)}$	≥	3.2	V 2) 3)
B-Y	$V_{7-16(p-p)}$	≥	4.0	V 2) 3)
G-Y	$V_{5-16(p-p)}$	≥	1.8	V 2) 3)
Impedance of chrominance inputs $V_{i(rms)}$ = 20 mV (sinusoidal); f = 4.4 MHz	$\lvert Z_{9-16}\rvert$ } $\lvert Z_{13-16}\rvert$ }	≥	800 Ω in parallel with 10 pF	

1) Ratio of peak to peak values of input and output signals.
2) Linearity ≥ 0.7 measured in the circuit on page 5.
3) Maximum output signal. For driving the TBA530 the input signal should be reduced by a factor 2.2.

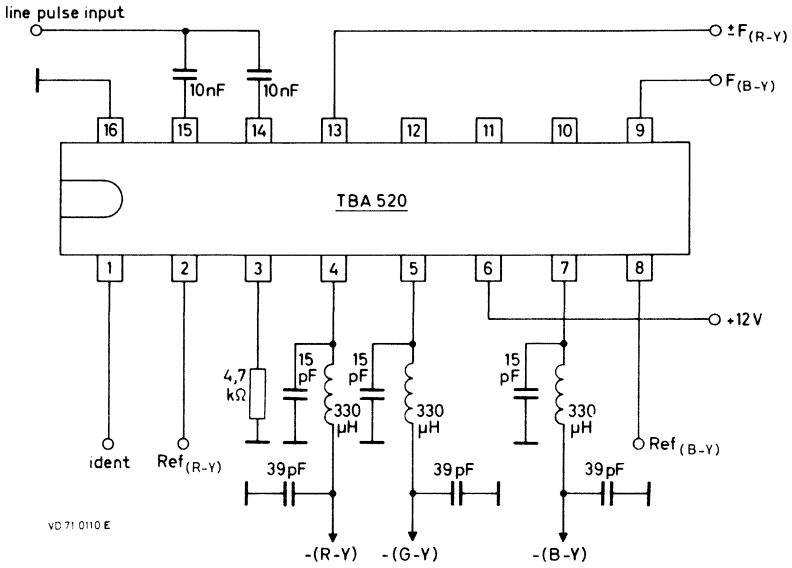
CHARACTERISTICS (continued)

Impedance of colour-difference signal outputs	$\|Z_{4-16}\|$	typ.	2.7	kΩ
	$\|Z_{7-16}\|$	typ.	2.7	kΩ
	$\|Z_{5-16}\|$	typ.	2.7	kΩ
Impedance of reference signal inputs	$\|Z_{2-16}\|$	typ.	1	kΩ
	$\|Z_{8-16}\|$	typ.	1	kΩ
Square wave output voltage peak to peak value; f = 7.8 kHz	$V_{3-16(p-p)}$	>	3	V
Input current				
Supply current consumption	I_6	typ.	32	mA
Input voltages				
Reference voltages (peak to peak values)				
at reference R-Y	$V_{2-16(p-p)}$	typ.	1	V
at reference B-Y	$V_{8-16(p-p)}$	typ.	1	V
Identification circuit active	I_1	≥	80	μA
	V_{1-16}	>	0.75	V
in-active	V_{1-16}	≤	0.4	V
Flip-flop drive pulses (15625 Hz; negative) peak to peak values	$V_{14-16(p-p)}$		3 to 4.5	V
	$V_{15-16(p-p)}$		3 to 4.5	V

PINNING

1. Identification bias
2. R-Y subcarrier reference input
3. P.A.L. square wave output (7.8 kHz)
4. R-Y signal output
5. G-Y signal output
6. Supply voltage (12 V)
7. B-Y signal output
8. B-Y subcarrier reference input
9. B-Y chrominance input signal
10. n.c.
11. G-Y d.c. level setting
12. R-Y d.c. level setting
13. R-Y chrominance input signal
14. Line pulse input (flip-flop synchronising)
15. Line pulse input (flip-flop synchronising)
16. Earth (negative supply)

APPLICATION INFORMATION



APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number (see also page 5).

1. Identification bias
The input current required to stop the flip-flop, "Ident on": $I_{on} \geq 80\ \mu A$.
For "Ident off": $V_{off} = -5$ to $+0.4$ V.

2. R-Y subcarrier reference input
An 1 V peak to peak signal is required via a d.c. blocking capacitor. Under no circumstances should this signal be less than 0.5 V peak to peak.
The input resistance at this pin lies between 670 Ω and 1250 Ω.
($y_{2-16} = 0.8$ to $1.5\ m\Omega^{-1}$)

3. P.A.L. square wave output
The amplitude is ≥ 3 V peak to peak from an emitter follower.

4. R-Y signal output (G-Y at pin 5 and B-Y at pin 7)
No external d.c. load needed except that direct connection must be made via the low pass filter to the R.G.B. matrix TBA530.

The signals produced are in the following ratios:

$$V_{B-Y} = 1.3\ V_{R-Y} \pm 10\%$$
(a) $V_{G-Y} = 0.76\ V_{R-Y} \pm 10\%$
(b) $V_{G-Y} = 0.26\ V_{R-Y} \pm 15\%$

Condition (a) refers to (B-Y) + (R-Y) addition in the G-Y matrix.
Condition (b) refers to the phase reversed (R-Y) input signal where (G-Y) is obtained by subtraction.

The d.c. levels should each be adjusted, starting with the (B-Y), to +7.5 V at nominal supply voltage.

The maximum peak to peak voltages for the condition $m \geq 0.7$ (m = ratio of minimum to maximum differential gains) are:

$$V_{R-Y(p-p)} \geq 3.2\ V$$
$$V_{G-Y(p-p)} \geq 1.8\ V$$
$$V_{B-Y(p-p)} \geq 4.0\ V$$

The output impedance for each signal is 2.7 kΩ.

The drifts in d.c. levels of the colour difference output signals for a change in ambient temperature of 40 °C (after equilibrium is reached from switch-on) are typically:

Absolute shift	−50 to +50 mV
V_{R-Y} relative to V_{B-Y}	−20 to +20 mV
V_{G-Y} relative to V_{B-Y}	−20 to +20 mV
V_{R-Y} relative to V_{G-Y}	−20 to +20 mV

APPLICATION INFORMATION (continued)

The changes in d.c. level with supply voltage are approximately linear and track together.

The −3 dB bandwidth of the colour difference signals is 1.5 MHz.

5. G-Y signal output (see pin 4)

6. L.T. positive supply
Also d.c. level setting for B-Y output (pin 7). The maximum allowable voltage on this pin is 13.2 V. The minimum supply voltage to ensure setting the B-Y output d.c. level correctly (+7.5 V) is 11.6 V (in such case RV_1 would be set to zero).

7. B-Y signal output (see pin 4)

8. B-Y subcarrier reference input
The requirements here are identical with those for pin 2.

9. Chrominance B-Y input signal

An input signal up to 360 mV peak to peak (colour bars) is allowed. For driving the TBA530 an input signal of 160 mV is required. The input impedance is greater than 800 Ω and the input capacitance is less than 10 pF (y_{9-16} and $y_{13-16} \leq 1.25$ m Ω^{-1} in parallel with 10 pF). The spread in gain of the internal circuitry in the chrominance channel is ±10 %.

10. Internally connected; no external connection should be made.

11. D.C. level setting for G-Y output signal (circuit diagram on page 5).

12. D.C. level setting for R-Y output (see circuit diagram on page 5).

13. Chrominance R-Y input signal
An input signal up to 500 mV peak to peak (colour bars) is allowed. The input impedance and spread in gain is the same as for pin 9.

14. Line pulse input (flip-flop synchronising)
A 4 V peak negative going line flyback pulse should be applied via separate 10 nF capacitors to pins 14 and 15. Pulse amplitude to lie between 3 V and 4.5 V peak to peak.

15. Line pulse input (see pin 14)

16. Negative supply (earth)

R.G.B. MATRIX PRE-AMPLIFIER

The TBA530 is an integrated circuit for colour television receivers incorporating a matrix pre-amplifier for R.G.B. cathode or grid drive of the picture tube without clamping circuits. The chip lay-out has been designed to ensure tight thermal coupling between all the transistors in each channel to minimise and equalise thermal drifts between channels. Also, each channel follows an identical lay-out to ensure equal frequency behaviour of the three channels.

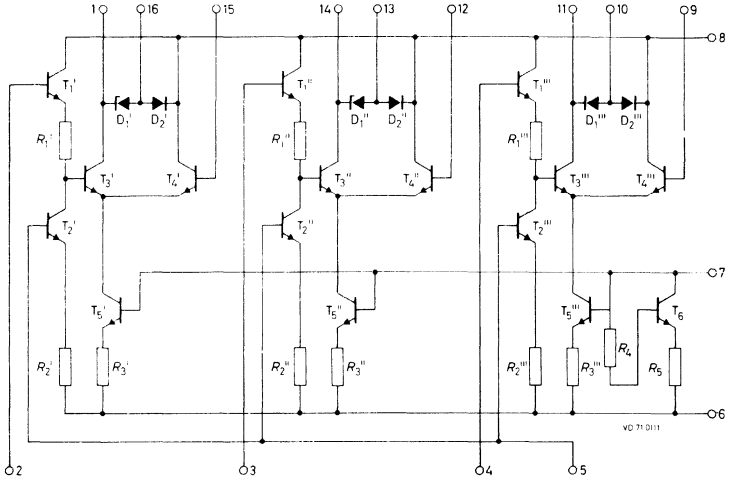
This integrated circuit has been designed to be driven from the TBA520 synchronous demodulator integrated circuit.

QUICK REFERENCE DATA				
Supply voltage	V_{8-6}	nom.	12	V
Ambient temperature	T_{amb}		25	°C
Gain of luminance and colour-difference channels	G	typ.	100	
Total current consumption	I_{tot}	typ.	30	mA

PACKAGE OUTLINE

TBA530 : 16 lead plastic dual in-line (type A) (See General Section).
TBA530Q: 16 lead plastic quadruple in-line (See General Section).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage				
Supply voltage	V_{8-6}	max.	13.2	V
Currents				
Supply currents	I_1 ; I_{11} ; I_{14}	max.	10	mA
	I_{10} ; I_{13} ; I_{16}	max.	50	mA[1])
Power dissipation				
Total power dissipation	P_{tot}	max.	400	mW[1])
Temperatures				
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		−20 to +60	°C

CHARACTERISTICS measured in circuit on page 5

Measuring conditions: V_{8-6} = 12 V; T_{amb} = 25 °C
black level: $V_{R-Y} = V_{G-Y} = V_{B-Y}$ = 7.5 V
V_Y = 1.5 V

Colour difference input peak-to-peak values	$V_{2-16(p-p)}$	typ.	1.4	V
	$V_{3-16(p-p)}$	typ.	1.78	V
	$V_{4-16(p-p)}$	typ.	0.82	V
Luminance input signal (peak-to-peak value)	$V_{5-16(p-p)}$	typ.	1	V
Gain of colour channels (B-Y;G-Y;R-Y) at f = 0.5 MHz	G_{2-6}, G_{3-6}, G_{4-6}	typ.	100	[2])
Ratio of gain of luminance amplifier to colour amplifiers		typ.	1	
D.C. output voltage	V_R, V_G, V_B	typ.	165	V

[1]) At increased voltages due to external failures (e.g. collector-basis breakdown in the output transistors) a maximum current of 50 mA is permitted between pins 16 and 8, 13 and 8, 10 and 8. The maximum allowable dissipation in this case is 500 mW.

[2]) G is defined as the voltage ratio between the input signals at the pins 2, 3, 4 and the output signals at the collectors of the output transistors.

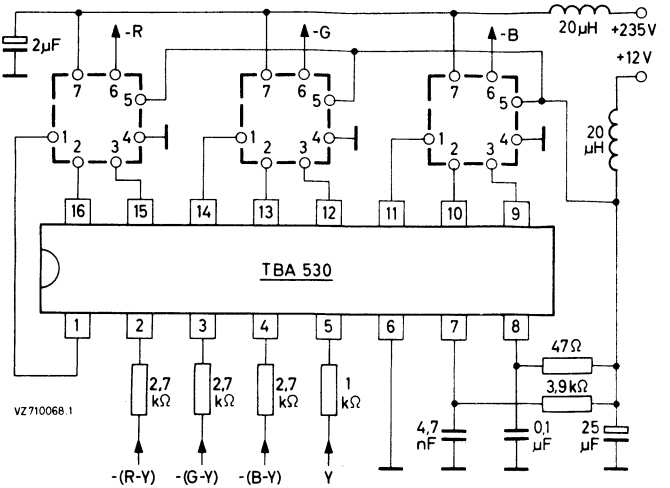
CHARACTERISTICS (continued)

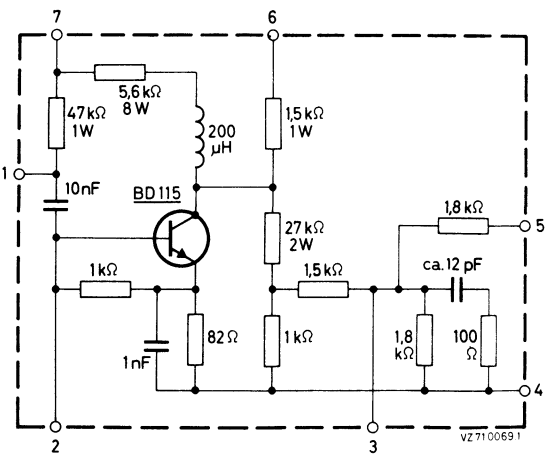
Input resistance of colour difference amplifiers at f = 1 kHz	R_{2-6} R_{3-6} R_{4-6}	typ.	60	kΩ
Input capacitance of colour difference amplifiers at f = 1 MHz	C_{2-6} C_{3-6} C_{4-6}	typ.	3	pF
Input resistance of luminance amplifier at f = 1 kHz	R_{5-6}	typ.	20	kΩ
Input capacitance of luminance amplifier at f = 1 MHz	C_{5-6}	typ.	10	pF
Bandwidth of all channels (3 dB)	B	typ.	6	MHz
Total current drain	I_{tot}	typ.	30	mA

PINNING see also APPLICATION INFORMATION circuit diagram on page 5.

1. Output load resistor (red signal)
2. R-Y input signal
3. G-Y input signal
4. B-Y input signal
5. Luminance signal input
6. Earth (negative supply)
7. Current feed point
8. 12 V positive supply
9. Blue channel feedback
10. Blue signal output
11. Output load resistor (blue signal)
12. Green channel feedback
13. Green signal output
14. Output load resistor (green signal)
15. Red channel feedback
16. Red signal output

APPLICATION INFORMATION





APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin numbering (see also page 5)

1. Output load resistor, red signal (pin 11: blue signal, pin 14: green signal)
Resistors (47 kΩ, 1 W) connected to +200 V provide the high value loads for the internal amplifying stages. The nominal operating potential on these pins is defined by an internal zener type junction and the d.c. feedback and is approximately +8 V. The maximum current which can be allowed at each of these pins is 10 mA.

2. R-Y input signal
This signal is fed via a low-pass filter from the TBA520 demodulator i.c. (pin 7) having a d.c. level of +7.5 V and an amplitude of 1.78 V peak to peak. The input resistance for this pin is typically 60 kΩ with an input capacitance of less than 3 pF (similarly for pins 3 and 4).

3. G-Y input signal
The d.c. black level of this signal is +7.5 V and its amplitude is 0.82 V peak to peak (see pin 2).

4. B-Y input signal
The d.c. black level of this signal is +7.5 V and its amplitude is 1.40 V peak to peak (see pin 2)

5. Luminance signal input
The d.c. level on this pin for picture black is +1.5 V. The required signal amplitude is 1 V black-to-white with negative-going sync (or blanking) for cathode drive as shown. The input resistance at this pin is 20 kΩ approximately with a capacitance of typ. 10 pF.

6. Negative supply (earth)

7. Current feed point
A current of approximately 2.5 mA is required at this pin, fed via a 3.9 kΩ resistor from +12 V, to bias the internal differential amplifiers. A decoupling capacitor of 4.7 nF is necessary.

8. Positive 12 V supply
Maximum supply voltage permitted, 13.2 V. Current consumption approximately 30 mA.

9. Blue channel feedback (green channel, pin 12: red channel, pin 15)
The d.c. working points and gains of both the output stages and the i.c. amplifier stages are stabilised by the feedback circuits. The black level potentials at the collectors of the output stages (tube cut-off) are adjusted by setting correctly the d.c. level of the colour difference signals produced by the TBA520 demodulator i.c. The gains of the R-G-B output stages are adjusted to give the correct white points setting on the picture tube by adjusting the potentiometers in the feedback paths (VR1, VR2). (See notes on setting up decoder).

APPLICATION INFORMATION (continued)

10. Blue signal output (green and red signal outputs on 13 and 16)
These pins are internally connected with pins 11, 14 and 1 respectively via zener type junctions to give a d.c. level shift appropriate for driving the output transistor bases directly. To by-pass the zener junctions at h.f. three 10 nF capacitors are required.

11. Output load resistor, blue channel (pin 1).

12. Green channel feedback (see pin 9).

13. Green signal output (see pin 10).

14. Output load resistor , green channel (see pin 1).

15. Red channel feedback (see pin 9).

16. Red signal output (see pin 10).

BRIEF PERFORMANCE DETAILS AND COMMENTS

1. Spread of the ratio of voltage gains for colour difference and luminance signal inputs 0.9 to 1.1.

2. Very careful attention to earth paths should be given, avoiding common impedances between the input (decoder) side and the output stages. Also, to enable matched performance to be achieved, a symmetrical board and component layout should be adopted for the three output stages. To compensate for the effect upon h.f. response of inevitable differences, e.g., the absence of a potentiometer in one of the stages, the compensating capacitors C_1, C_2 and C_3 may be appropriately selected for any given board layout.

3. The signal black level at the collectors of the R-G-B output stages depends upon the +12 V supply, the d.c. level of the colour difference signals from the TBA520 demodulator i.c. and the black level potential of the luminance signal applied to the TBA530 matrix i.c. The d.c. levels of the signals produced and handled by the i.c.'s are designed to have approximately proportional tracking with the 12 V supply potential,

$$\text{i.e., } \frac{\Delta V_{(\text{d.c. level, signal})}}{\Delta V_{12V}} \approx \frac{V_{\text{nom(d.c. level, signal)}}}{12}$$

To ensure that changes in picture black level due to variations on the 12 V supply to the i.c.'s occur in a predictable way, all the i.c.'s should be operated from a common supply line. This is specially important for the TBA520 and TBA530. Furthermore, to limit the changes in picture black level during receiver operation, the 12 V supply should have a stability of not worse than ±3% due to operational variations, and preferably be tracked with the screen-grid supply of the picture tube.

REFERENCE COMBINATION

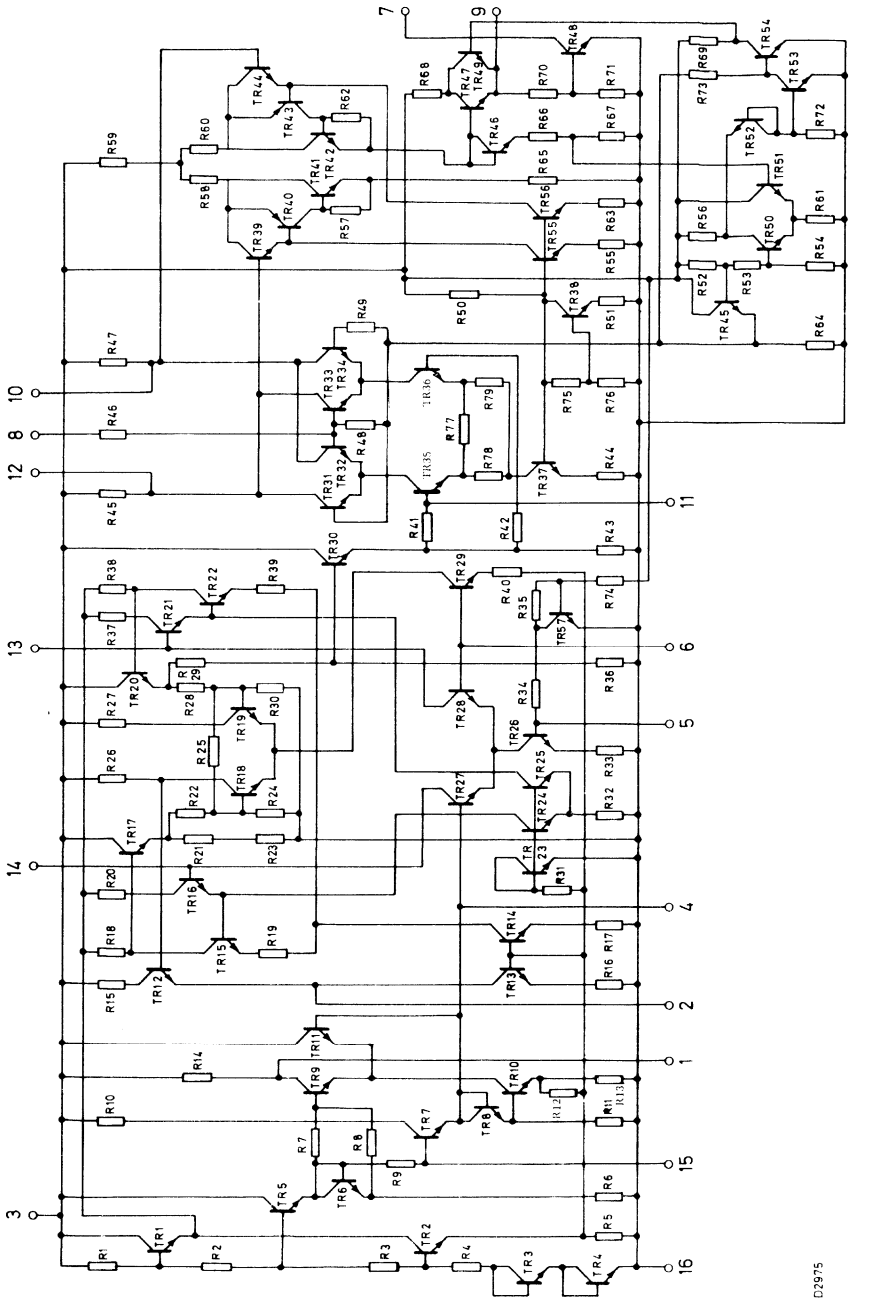
The TBA540 is an integrated reference oscillator circuit for colour television receivers incorporating an automatic phase and amplitude controlled oscillator employing a quartz crystal, together with a half-line frequency synchronous demodulator circuit. The latter compares the phases and amplitude of the swinging burst ripple and the P.A.L. flip-flop waveform, and generates appropriate a.c.c., colour killer and identification signals. The use of synchronous demodulation for these functions permits a high standard of noise immunity.

QUICK REFERENCE DATA				
Supply voltage	V_{3-16}	nom.	12	V
Total current drain	I_3	typ.	33	mA
R-Y reference signal output				
peak-to-peak value	$V_{4-16(p-p)}$	typ.	1.5	V
Colour killer output: colour on	V_{7-16}	typ.	12	V
colour off	V_{7-16}	<	250	mV
A.C.C. output voltage range				
at correct phase of P.A.L. switch	V_{9-16}		+4 to +0.2	V
at incorrect phase of P.A.L. switch	V_{9-16}		+4 to +11	V

PACKAGE OUTLINE

TBA540 : 16 lead plastic dual in-line (type A) (See General Section).
TBA540Q: 16 lead plastic quadruple in-line (See General Section).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage				
Supply voltage	V_{3-16}	max.	13.2	V
Power dissipation				
Total power dissipation at T_{amb} = 50 °C	P_{tot}	max.	680	mW
Temperatures				
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		−20 to +60	°C

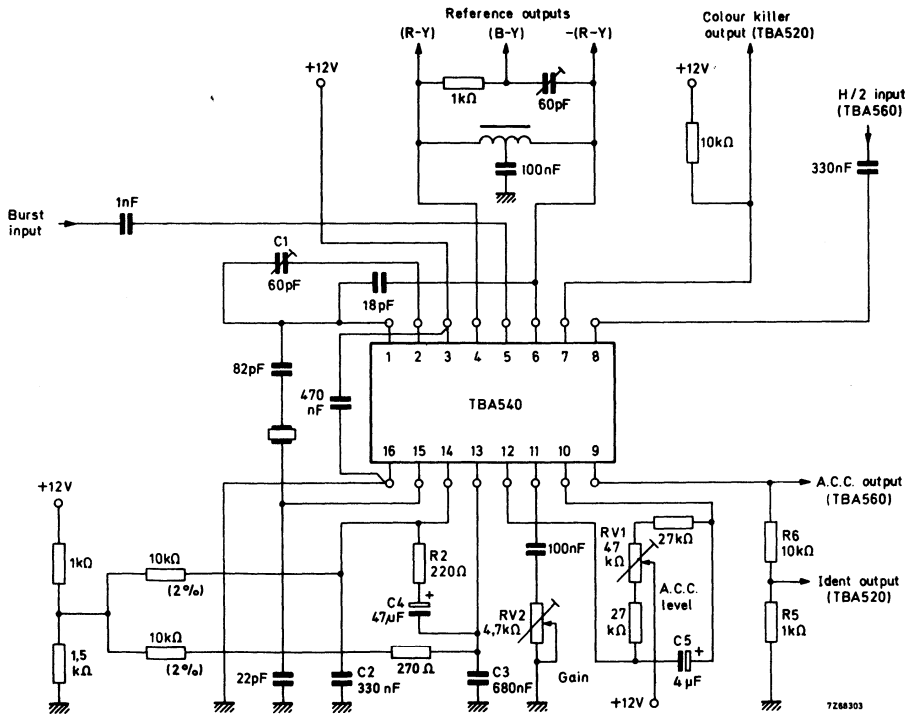
CHARACTERISTICS at V_{3-16} = 12 V; T_{amb} = 25 °C; V_{5-16} $\dot{M}$ = 0.7 V (burst signal input); $V_{8-16(p-p)}$ = 2.5 V (P.A.L. square wave input) Measured in circuit shown on page 4.

Output signals				
R-Y reference signal output peak-to-peak value	$V_{4-16(p-p)}$	typ.	1.5	V
Colour killer output: colour on	V_{7-16}	typ.	12	V
colour off	V_{7-16}	<	250	mV
A.C.C. output signal range				
at correct phase of P.A.L. switch	V_{9-16}		+4 to +0.2	V
at incorrect phase of P.A.L. switch	V_{9-16}		+4 to +11	V
Oscillator section (amplifier)				
Input resistance	R_{15-16}	typ.	3.5	kΩ
Input capacitance	C_{15-16}	typ.	5	pF
Voltage gain	G_{15-1}	typ.	4.7	
Reactance control section				
Voltage gain with pins 13 and 14 interconnected	G_{15-2}	typ.	1.3	
Rate of change of gain G_{15-2} with phase difference between burst and reference signal	$\frac{\Delta G_{15-2}}{\Delta \varphi_{5-4}}$	typ.	5	$\frac{1}{rad}$
Supply current consumption	I_3	typ.	33	mA

PINNING

1. Oscillator feedback output
2. Reactance control stage feedback
3. Supply voltage (12 V)
4. Reference waveform output
5. Burst waveform input
6. Reference waveform input
7. Colour killer output
8. P.A.L. flip-flop square wave input
9. A.C.C. output
10. A.C.C. level setting (see also pin 12)
11. A.C.C. gain setting
12. A.C.C. level setting (see also pin 10)
13. } D.C. control points for
14. } oscillator phase control loop
15. Oscillator feedback input
16. Earth (negative supply)

APPLICATION INFORMATION



APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Oscillator feedback output
   The crystal receives its energy from this pin. The input impedance is approximately 2 kΩ in parallel with 5 pF.

2. Reactance control stage feedback
   This pin is fed internally with a sinewave derived from the reference input (pin 6) and controlled in amplitude by the internal reactance control circuit. The phase of the feedback from pin 2 to the crystal via C1 is such that the value of C1 is effectively increased. Pin 2 is held internally at a very low impedance therefore the tuning of the crystal is controlled automatically by the amplitude of the feedback waveform and its influence on the effective value of C1.

3. Positive 12 V supply
   The maximum voltage must not exceed 13.2 V.

4. Reference waveform output
   This pin is driven internally by the regenerated subcarrier waveform in R-Y phase. An output amplitude of nominally 1.5 V peak-to-peak is produced at low impedance. No d.c. load to earth is required. A d.c. connection between pins 4 and 6 is, however, necessary via the bifilar coupling inductor. The function of this inductor is to produce, on pin 6, a signal of equal amplitude and opposite phase (-(R-Y)) to that on pin 4. A centre tap on the inductor, connected to earth via a d.c. blocking capacitor, is therefore necessary.

5. Burst waveform input
   A burst waveform amplitude of 1 V peak-to-peak is required to be a.c.-coupled to this pin. The amplitude of the burst will normally be controlled by the adjustment and operation of the a.c.c. circuit. The input impedance at this pin is approximately 1 kΩ and a threshold level of 0.7 V must be exceeded before the burst signal becomes effective. A d.c. bias of 400 mV is internally derived for pin 5 The absolute level of the tip of the burst at pin 5 will normally reach 1.25 V (1.5 V peak-to-peak burst amplitude). Under abnormal conditions the burst amplitude should not be allowed to exceed 3 V peak-to-peak and a limiting condition will be reached in the i.c. which inhibits the performance of the phase lock loop.

APPLICATION INFORMATION (continued)

6. Reference waveform input
This pin requires a reference waveform in the -(R-Y) phase, derived from pin 4 via a bifilar transformer (see pin 4), to drive the internal balanced reactance control stage. A d.c. connection between pins 4 and 6 must be made via the transformer.

7. Colour killer output
This pin is driven from the collector of an internal switching transistor and requires an external load resistor (typical 10 kΩ) connected to +12 V. The unkilled and killed voltages on this pin are then +12 V and < 250 mV respectively. (The voltage on pin 9 at which switching of the colour killer output on pin 7 occurs is nominally +2.5 V

8. P.A.L. flip-flop square wave input
A 2.5 V peak-to-peak square wave derived from the P.A.L. flip-flop (in the TBA520 demodulator i.c.) is required at this pin, a.c.-coupled via a capacitor. The input impedance is about 3.3 kΩ.

9. A.C.C. output
An emitter follower provides a low impedance output potential which is negative-going with a rising burst input amplitude. With zero input signal the d.c. potential produced at pin 9 is set to be +4 V (RV1) The appearance of a burst signal on pin 5 will cause the potential on pin 9 to go in a negative direction in the event that the P.A.L. flip-flop is identified to be in the correct phase. The range of potential over which full a.c.c. control is excercised at pin 9 is determined by the control characteristics of the a.c.c. amplifier i.e. for the TBA560 from 1 V to 0.2 V. The potential at pin 9 will fall to a value within this range as the burst input signal is stabilised at 1.5 V peak-to-peak. The latter condition is achieved by correct adjustment of RV2. If, however, the P.A.L. flip-flop phase is wrong the potential on pin 9 will move positively. The potential divider R5, R6 will then operate a P.A.L. switch cut-off function in the TBA520 demodulator i.c. The switching of the colour killer output at pin 7 is designed to occur as the potential on pin 9 moves past +2.5 V.

10. A.C.C. level setting
The network connected between pins 10 and 12 balances the a.c.c. circuit and RV1 is adjusted to give +4 V on pin 9 with no burst input signal to pin 5. C5 provides filtering.

11. A.C.C. gain control
RV2 is adjusted to give the correct amplitude of burst signal on pin 5 (1.5 V peak-to-peak) under a.c.c. control;

12. See pin 10.

13. See pin 14.

APPLICATION INFORMATION (continued)

14. D.C. control points in reference control loop
Pins 13 and 14 are connected to opposite sides of a differential amplifier circuit and are brought out for the purposes d.c. balancing of the reactance stage and the connection of the bandwidth-determining filter network. The conventional double time constant filter networks are R2, C2, R3, C3 and R_4, C_4. The d.c. potentials on these pins are nominally +7,2 V.

15. Oscillator feedback input
The input impedance at this pin is nominally 3.5 kΩ in parallel with 5 pF. No d.c. connection is required on this pin. The voltage in the i.c. between pin 15 and pin 1 is nominally 4.7 times.

16. Negative supply (earth)

PERFORMANCE AND COMMENTS

Initial adjustment

(a) Remove burst signal.

(b) Short-circuit pins 13-14. Adjust oscillator to correct frequency by C1. Remove short circuit.

(c) Set the a.c.c. level adjustment RV1, to give +4 V on pin 9.

(d) Apply burst signal.

(e) Adjust a.c.c. gain, RV2, to give a burst amplitude of 1.5 V peak-to-peak on pin 5.

Phase lock loop performance (with crystal type 4322 152 0110)

(a) Phase difference between reference and burst signals for ±400 Hz deviation of crystal frequency, ± 10^{o}.

(b) Typical holding range, ± 600 Hz.

(c) Typical pull-in range, ± 300 Hz.

(d) Temperature coefficient of oscillator frequency, i.c. only, 2 Hz/^{o}C.

TELEVISION SIGNAL PROCESSING CIRCUIT

The TBA550 is a silicon monolithic integrated signal processing circuit for television receivers. It combines following functions:

- video pre-amplifier with emitter follower output
- gated a.g.c. detector supplying the a.g.c. voltages for the vision i.f. amplifier and tuner (delayed)
- noise inverter for gating the a.g.c. and sync separator circuits
- sync separator
- automatic horizontal synchronisation
- vertical sync pulse separator
- blanking facility for the video amplifier

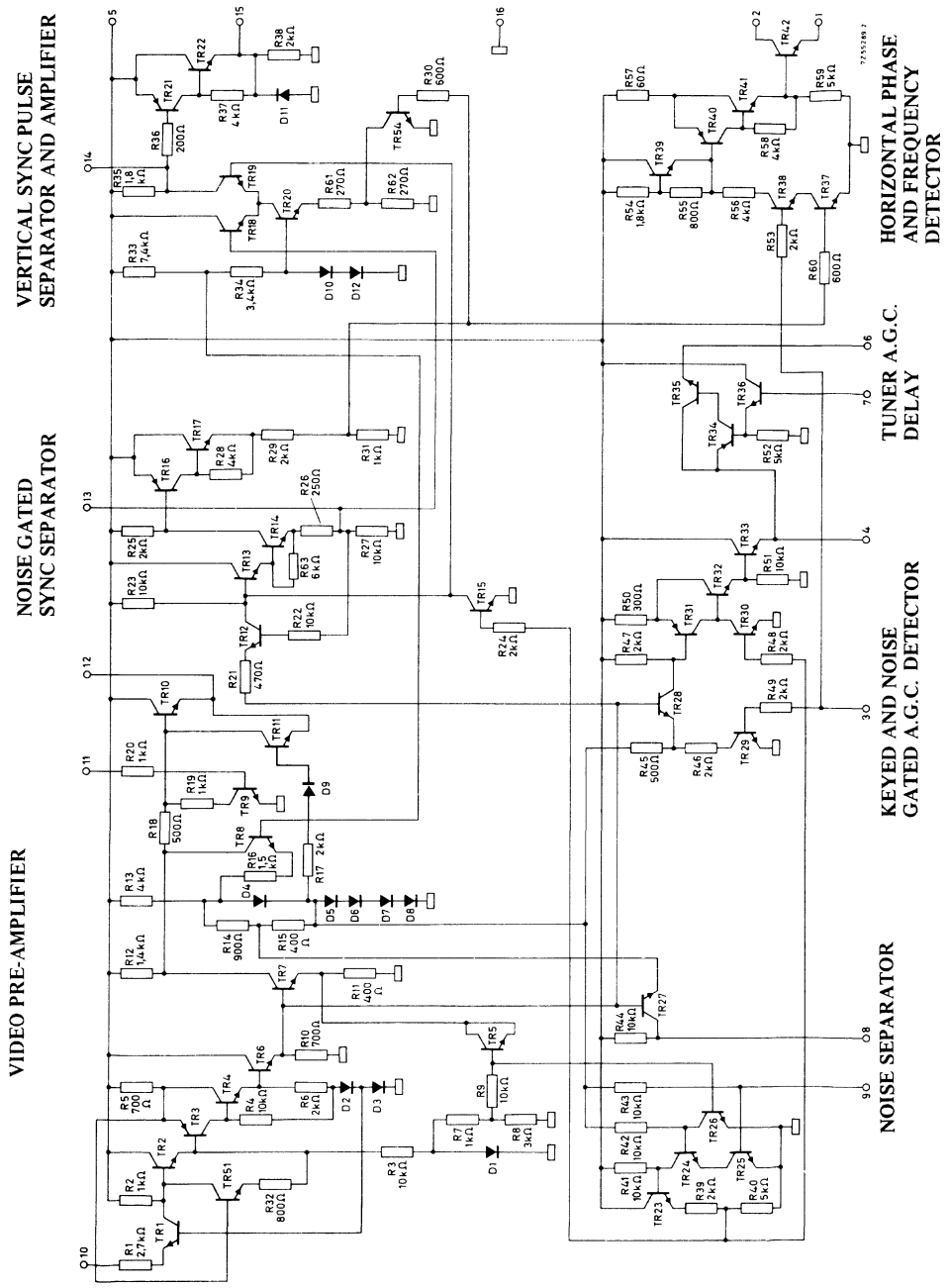
The circuit is designed for receivers equipped with tubes or transistors in the deflection and video output stages, and with n-p-n transistors in the tuner and i.f. amplifier. Only signals with negative modulation can be handled by the circuit.

QUICK REFERENCE DATA				
Supply voltage	V_P	typ.	12	V
Ambient temperature	T_{amb}		25	°C
Video input voltage (peak-to-peak voltage)	$V_{10-16(p-p)}$	typ.	2	V
Voltage gain of the the video amplifier	G_v	typ.	9,5	dB
A.G.C. voltage for i.f. part (R_{4-16} = 2 kΩ)	V_{4-16}	typ.	0 to 8	V
A.G.C. voltage for tuner (R_{6-16} = 1 kΩ)	V_{6-16}	typ.	0 to 7	V
Output voltage horizontal phase detector	$\pm V_{2-1}$	typ.	3	V
Vertical sync output voltage (positive going pulse; peak-to-peak value)	$V_{15-16(p-p)}$	>	10	V

PACKAGE OUTLINE

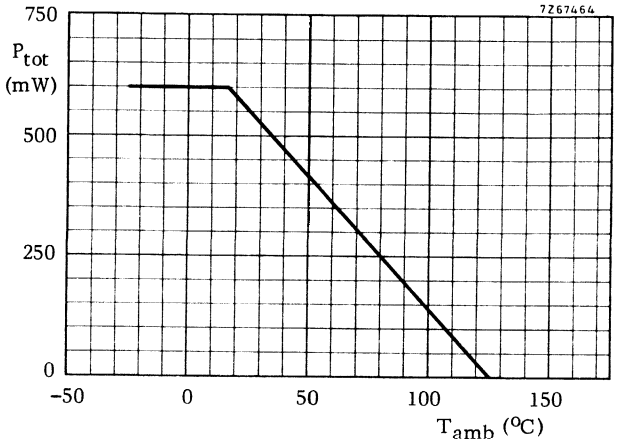
TBA550 : 16 lead plastic dual in-line (type A) (See General Section)
TBA550Q: 16 lead plastic quadruple in-line (See General Section)

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	16	V [1])
Power dissipation	P_{tot}	max.	600	mW



Temperatures

Storage temperature	T_{stg}	-25 to +125	°C
Ambient temperature	T_{amb}	-25 to +125	°C

[1]) Permissible while tubes are heating up.

CHARACTERISTICS

Supply voltage range	V_P		10 to 14	V	
Measured in circuit on page 6 at T_{amb} = 25 °C; V_P = 12 V					
Video amplifier					
Input resistance (detector load)	R_{10-16}	typ.	2,7	kΩ	
Input capacitance	C_{10-16}	<	1	pF	
Bandwidth (3 dB)	B	.>	5	MHz	
Voltage gain	G_v	typ.	9,5	dB	
Video input voltage (peak-to-peak value)	$V_{10-16(p-p)}$	typ.	2	V	1)
Video output voltage (peak-to-peak value)	$V_{12-16(p-p)}$	typ.	5,2	V	2)
Tolerances on video output voltage:					
I.C. processing spreads	$\pm\Delta V_{12-16}$	<	550	mV	
Temperature drift	$-\Delta V_{12-16}$	<	20	mV/°C	3)
Spreads over a.g.c. expansion (entire range)	$\pm\Delta V_{12-16}$	<	270	mV	4)
Black level at the output	V_{12-16}	typ.	5	V	5)
Tolerances on the black level at the output					
I.C. processing spreads	$\pm\Delta V_{12-16}$	<	300	mV	
Temperature drift	ΔV_{12-16}	<	7	mV/°C	3)
Spreads over a.g.c. expansion (entire range)	$\pm\Delta V_{12-16}$	<	250	mV	4)6)
Variation black level at the output due to supply voltage variations	$\frac{\Delta V_{12-16}}{\Delta V_P}$	typ.	0,7		
Available video output current (peak value)	I_{12M}	typ.	14	mA	7)

1) Negative going video signal (no pre-bias needed for the detector).
2) Video signal with negative going sync pulse.
3) Because the integrated circuit reaches 95% of its final working temperature in 100 seconds, the temperature variations to be considered are those caused by the slower rise in cabinet temperature and by changes in room temperature.
4) Variation about a nominal condition, the i.f. being fully controlled and the tuner uncontrolled. The video signal increases and the black level decreases with increasing antenna signal.
5) Only valid if the video signal is in accordance with the CCIR standard.
6) To this must be added 0,7 ΔV_P, if operation of the a.g.c. causes a change in V_P.
7) The total load on pin 12 must be such that under nominal conditions $I_{12M} \leq 14$ mA.

CHARACTERISTICS (continued)

Video blanking					
Input voltage (peak-to-peak value)	$V_{11-16(p-p)}$		1 to 5	V	
Input resistance	R_{11-16}	typ.	1	kΩ	
A.G.C. circuit					
Control voltage i.f. amplifier	V_{4-16}		0 to 8	V	1)
Control voltage tuner	V_{6-16}		0 to 7	V	1)
Signal expansion for full control of i.f. amplifier and tuner		<	15	%	1)
Keying input pulse (peak-to-peak value)	$V_{3-16(p-p)}$		1 to 5	V	2)
Input resistance	R_{3-16}	typ.	1	kΩ	
Synchronisation circuit					
Sync separator		see note 3			
Control voltage line oscillator	$\pm V_{2-1}$	typ.	3	V	4)
Output voltage vertical sync pulse separator (peak-to-peak value)	$V_{15-16(p-p)}$	>	10	V	
Output impedance	R_{15-16}	typ.	2	kΩ	

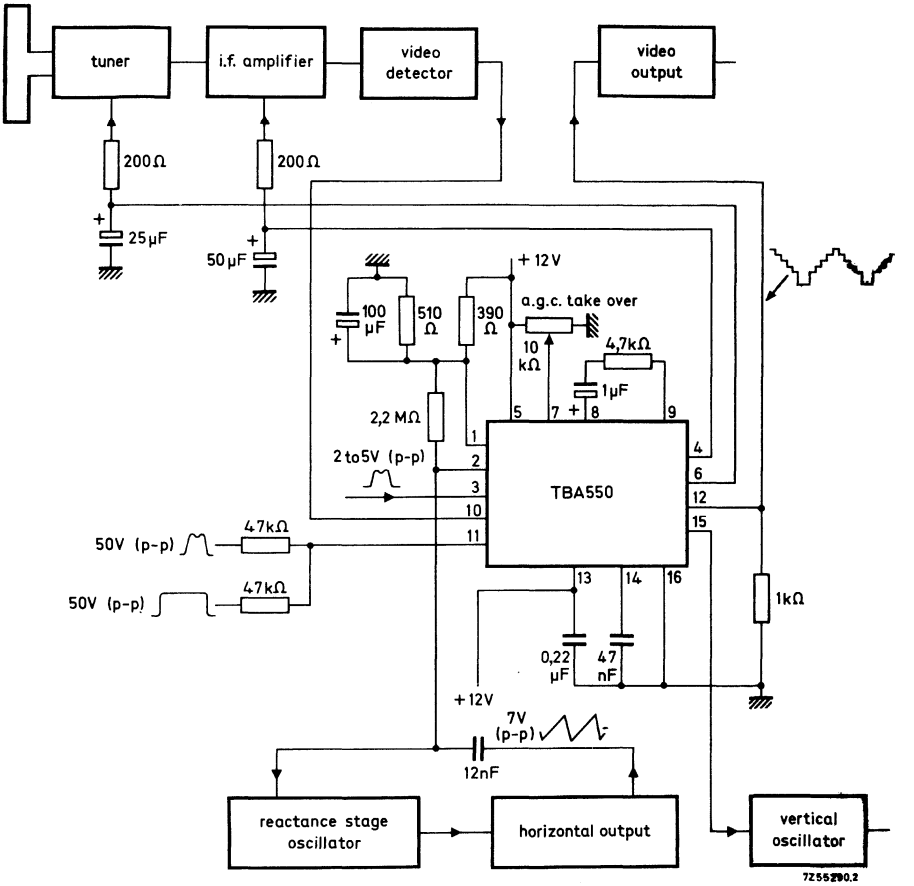
1) These figures are obtained with a load impedance of 2 kΩ for the i.f. control point (R_{4-16}) and 1 kΩ for the tuner control point (R_{6-16}). With these impedances the signal exapnsion for i.f. control and tuner control will be about the same. An in-increase of these impedances will reduce the signal expansion. Lower values will reduce the available control voltage and increase the dissipation of the integrated circuit. Therefore, the minimum values must be restricted to 1,5 kΩ for the i.f. control point and 750 Ω for the tuner control point.

2) The TBA550 may be operated unkeyed but then pin 3 must be connected to the positive supply line via a resistor of suitable value (e.g. 10 kΩ). However, the following consequences should be borne in mind:
- The decoupling capacitors at the i.f. and tuner control points must be larger to prevent ripple voltages due to the vertical sync pulses. In consequence the a.g.c. will not follow fast signal fluctuations (airplane flutter).
- Since the horizontal phase detector is designed to be keyed, unkeyed operation will result in the phase detector not operating as a frequency detector when the horizontal oscillator is out of of sync. This considerably decreases the catching range.

3) The sync pulse is sliced about 30% below top sync level.

4) Required reference voltage $V_{2(p-p)}$ (sawtooth or differentiated line fly-back pulse) = 7 V. For an oscillator-reactance stage with a control sensitivity of 400 Hz/V this gives a holding range of about ±1000 Hz.
Because the phase detector is keyed a catching range of ±700 Hz is obtained without affecting the noise immunity.

APPLICATION INFORMATION



LUMINANCE AND CHROMINANCE CONTROL COMBINATION

The TBA560B is a monolithic integrated circuit used in the decoding system of colour television receivers. The circuit consists of a luminance and a chrominance amplifier.
The luminance amplifier input is matched to the luminance delay line and performs the following functions:
d.c. contrast control * brightness control * black level clamping * blanking

The chrominance amplifier comprises:
gain-controlled amplifier * chrominance gain control tracked with contrast control * separate d.c. saturation control * P.A.L. delay line driver * burst gate * colour killer.
Compared with the TBA560C the TBA560B produces less gain of the burst signal and consequently a larger ratio of the chrominance output signal to the burst output signal.

QUICK REFERENCE DATA

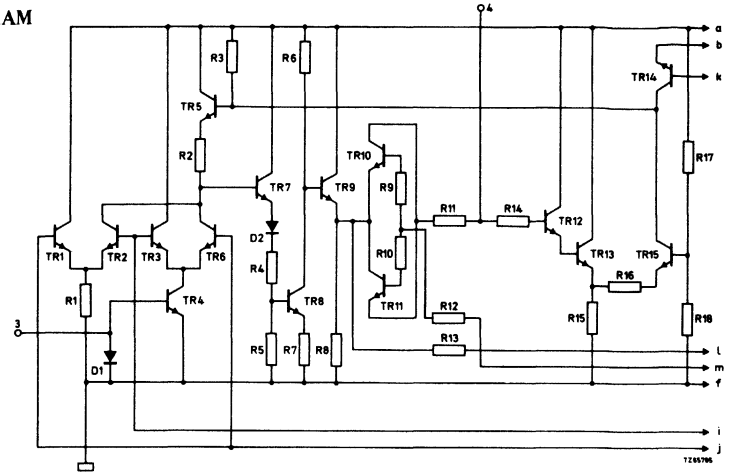
Supply voltage	$V_{11\text{-}16}$	nom.	12	V	
Supply current	I_{11}	nom.	30	mA	
Luminance signal input current	$I_{3(p\text{-}p)}$	typ.	1,5	mA	
Chrominance input signal	$V_{1\text{-}15(p\text{-}p)}$	>	6	mV	
		<	120	mV	
Luminance output signal at nominal contrast setting	$V_{5\text{-}16(p\text{-}p)}$	typ.	3	V	[1]
Chrominance output signal at nominal contrast and saturation setting	$V_{9\text{-}16(p\text{-}p)}$	typ.	2	V	[1]
Contrast control range		≥	20	dB	
Saturation control range		≥	20	dB	
Burst output (closed a.c.c. loop)	$V_{7\text{-}16(p\text{-}p)}$	typ.	1	V	

[1]) Nominal setting: maximum contrast and/or saturation minus 6 dB

PACKAGE OUTLINE

TBA560B : 16 lead plastic dual in-line (type A) (See General Section)
TBA560BQ: 16 lead plastic quadruple in-line (See General Section)

CIRCUIT DIAGRAM



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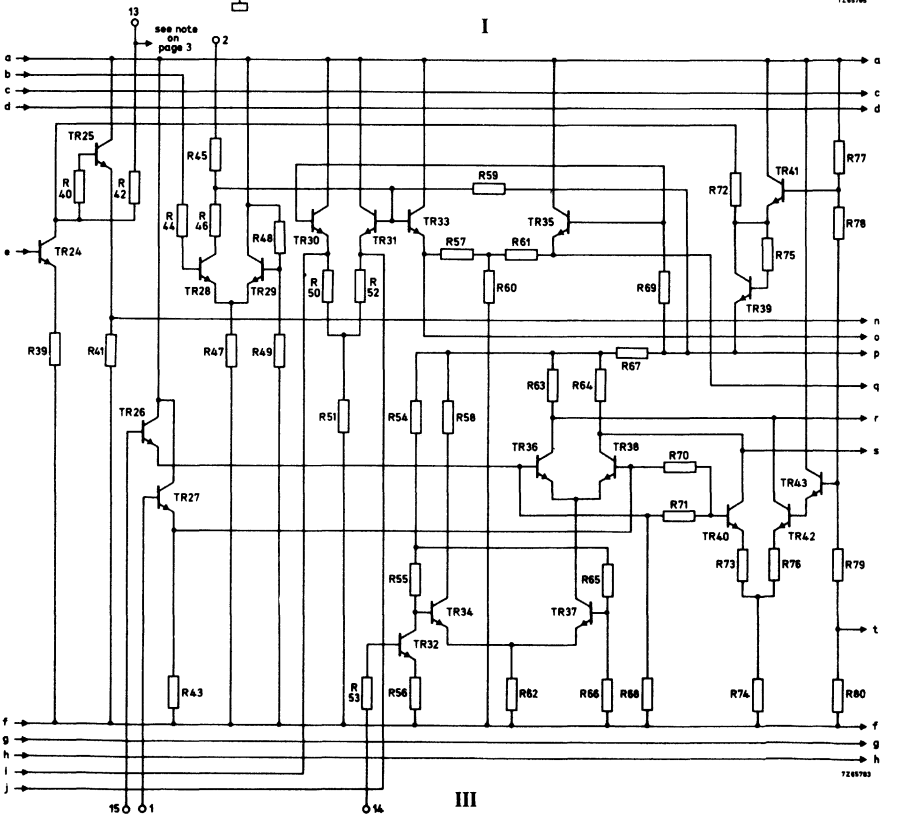
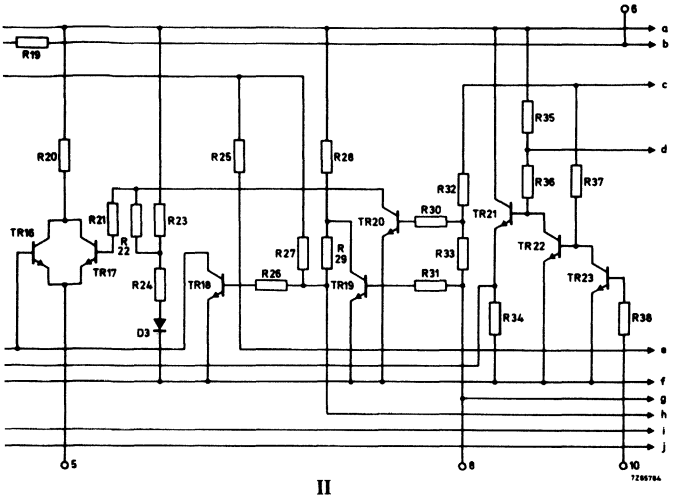
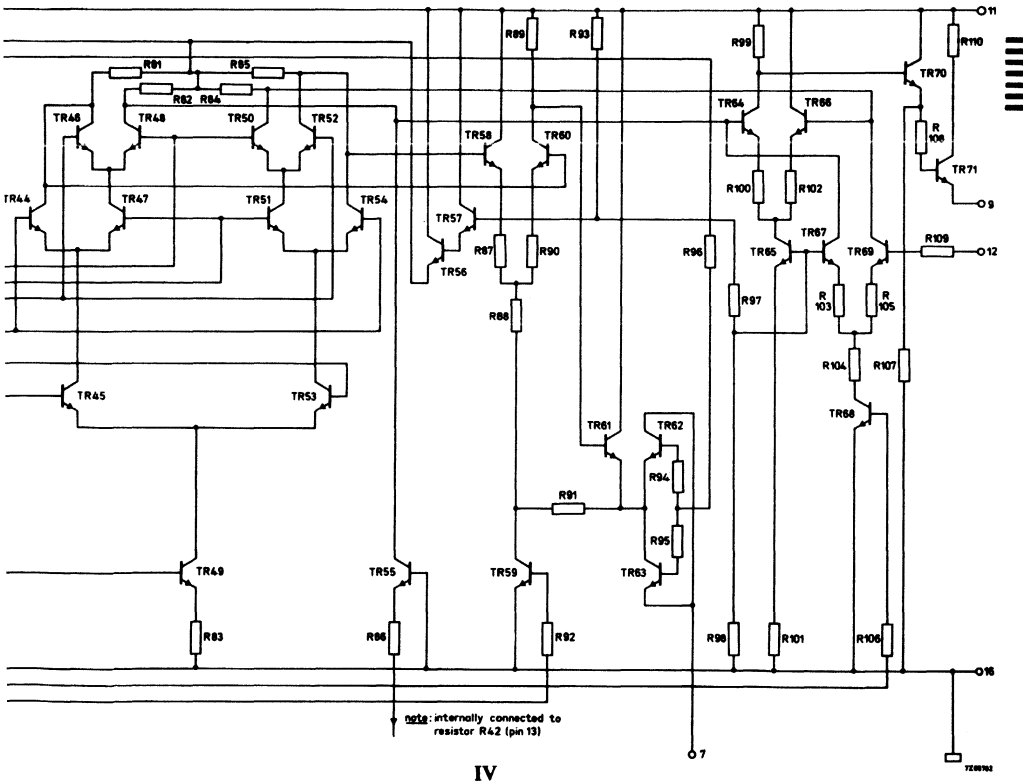


III

Note: the circuits are interconnected in the numerical sequence I, II, III, IV


R19
R20
R25
R28
R35
R36
R37
R32
R30
R21
R22
R23
TR16
TR17
TR20
TR21
TR22
R27
R29
R33
R24
TR18
R26
TR19
R31
TR23
D3
R34
R38
a
b
c
d
e
f
g
h
i
j
6
5
8
10
TZ86784

II


R91
R95
R92
R94
TR48
TR48
TR50
TR52
TR44
TR47
TR51
TR54
TR45
TR53
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R93
TR58
TR60
TR57
TR56
R87
R90
R88
R96
R99
TR64
TR66
R100
R102
TR67
TR65
TR69
R97
R103
R105
R104
R107
TR68
TR70
R110
R108
TR71
R109
11
9
12
TR61
TR62
R94
R91
R95
TR49
TR55
TR59
TR63
R83
R86
R92
R98
R101
R106
16
7
note: internally connected to resistor R42 (pin 13)
TZ86783

IV

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage	V_{11-16}	max.	13	V [1]

Power dissipation

Total power dissipation	P_{tot}	max.	510	mW [1]

Temperatures

Storage temperature	T_{stg}	−25 to +125	°C
Operating ambient temperature	T_{amb}	0 to +60	°C

Voltages with respect to pin 16

V_{1-16}	0 to +5 V	V_{10-16}	min. −5 V
V_{2-16}	0 to +12 V [2]	V_{12-17}	−5 to +6 V
V_{4-16}	0 to +6 V	V_{13-16}	−3 to +6,5 V [2]
V_{6-16}	0 to +3 V	V_{14-16}	min. −5 V
V_{8-16}	−5 to +5 V	V_{15-16}	0 to +5 V

Currents (positive when flowing into the integrated circuit)

I_1	0 to +1 mA	I_7	−3 to +2 mA
I_3	−1 to +3 mA	I_9	−10 to 0 mA
I_5	−5 to 0 mA	I_{10}	max. +3 mA
I_6	−1 to +1 mA	I_{14}	max. +1 mA
		I_{15}	0 to +1 mA

[1]) Permissible while tubes are heating up: V_{11-16} max. 16 V and P_{tot} max. 700 mW.

[2]) V_{2-16} and V_{13-16} must always be lower than V_{11-16}.

CHARACTERISTICS measured in the circuit on page 6

Supply voltage	V_{11-16}	typ.	12	V
			10 to 13	V

Required input signals at V_{11-16} = 12 V and T_{amb} = 25 °C

Chrominance input signal				
peak-to-peak value	$V_{1-15(p-p)}$		6 to 120	mV
Luminance input current				
black-to-white value	I_3	typ.	1,5	mA
Contrast control voltage range				
for 20 dB of control	V_{2-16}	see graph on page 11		
Brightness control voltage	V_{6-16}	see graph on page 11		[1]
Saturation control voltage range				
for 20 dB of control	V_{13-16}	see graph on page 11		
Burst keying pulse (positive)				
peak-to-peak value	$I_{10(p-p)}$		0,05 to 1	mA
Flyback blanking pulses (negative)				
peak-to-peak value				
for 0 V blanking level at pin 5	$V_{8-16(p-p)}$	typ.	−0,5	V
for 1,5 V blanking level at pin 5	$V_{8-16(p-p)}$	typ.	−2,5	V
Colour killer	V_{13-16}	<	1	V
Automatic chrominance control starting	V_{14-16}	typ.	1,2	V [2]

[1] When V_{6-16} is increased above 1,7 V the black level of the output signal remains at 2,7 V.

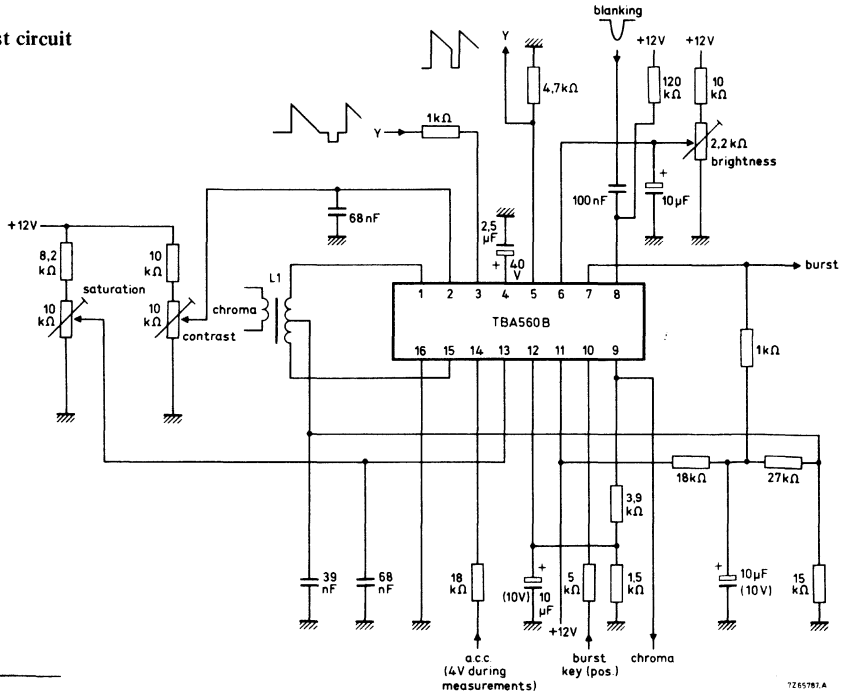
[2] A negative going potential provides a 26 dB a.c.c. range with negligible signal distortion. Maximum gain reduction is obtained at an input voltage of min. 500 mV.

CHARACTERISTICS (continued)

Obtainable output signals

Luminance output voltage at nominal contrast (peak-to-peak value)	$V_{5\text{-}16(p\text{-}p)}$	typ.	3	V	1)
Burst signal (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$	typ.	1	V	2)
Chrominance signal at nominal contrast and saturation (peak-to-peak value)	$V_{9\text{-}16(p\text{-}p)}$	typ.	2	V	1)
3 dB bandwidth of chrominance and luminance amplifier	B	typ.	5	MHz	
Change of ratio luminance to chrominance signals at 10 dB contrast control		<	2	dB	

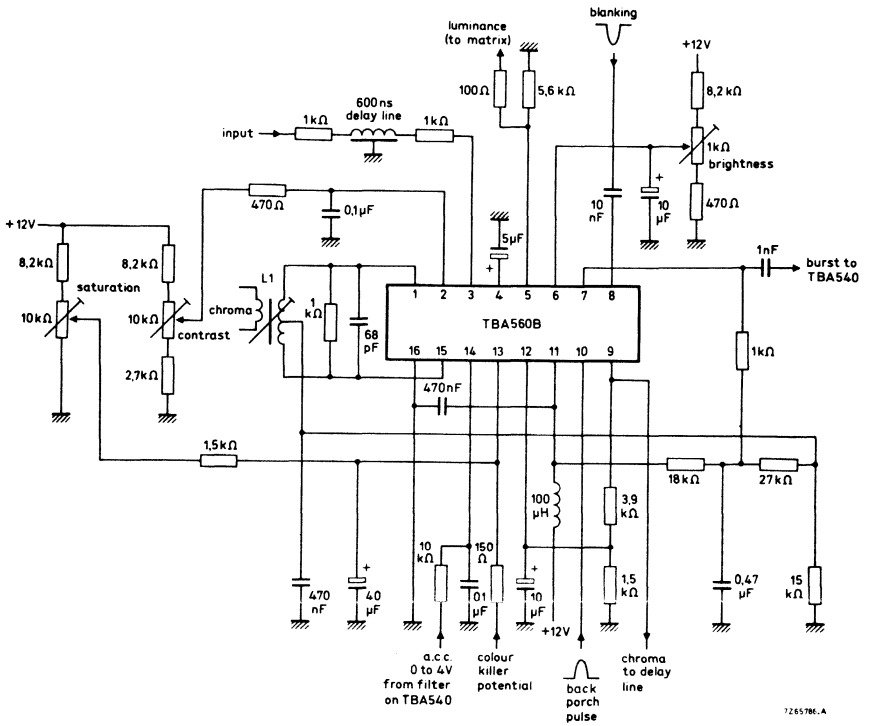
Test circuit



1) Nominal setting: maximum contrast and/or saturation minus 6 dB.

2) Burst signal is kept constant at 1 V peak-to-peak by automatic gain control.

APPLICATION INFORMATION



Application diagram for operation in combination with the TBA540

APPLICATION INFORMATION (continued)

Pinning

1.	Balanced chroma signal input	9.	Chroma signal output
2.	Contrast control	10.	Burst gate and clamping pulse input
3.	Luminance signal input	11.	Supply voltage (12 V)
4.	Black level clamp capacitor	12.	D.C. feedback for chroma channel
5.	Luminance signal output	13.	Chroma saturation control
6.	Brightness control	14.	A.C.C. input
7.	Burst output	15.	Chroma signal input
8.	Fly-back blanking input	16.	Earth (negative supply)

The function is quoted against the corresponding pin number

1. Balanced chroma signal input (in conjunction with pin 15)

   This is derived from the chroma signal bandpass filter, designed to provide the push-pull input. An input signal amplitude of at least 6 mV peak-to-peak is required on pins 1 and 15. Both pins require a d.c. potential of approximately +3,0 V. This is derived as a common-mode signal from a network connected to pin 7 (burst output). In this way d.c. feedback is provided over the burst channel to stabilise its operation.
   All figures for the chrominance signals are based on a colour bar signal with 75% saturation: i.e. burst-to-chroma ratio of input signal is 1 : 2.

2. D.C. contrast control

   With +3,7 V on this pin, the gain in the luminance channel is such that a 1,5 mA peak-to-peak input signal to pin 3 gives a luminance output signal amplitude on pin 5 of 3 V black-to-white. A variation of voltage on pin 2 between +6 V and +2 V gives a corresponding gain variation of +6 to > −14 dB. A similar variation in gain in the chroma channel occurs in order to provide the correct tracking between the two signals.

3. Luminance signal input

   This terminal has a very low input impedance and acts as a current sink. The luminance signal from the delay line is fed via a series terminating resistor and must have about 1,5 mA black-to-white amplitude.

4. Charge storage capacitor for black level clamp (5,0 μF)

5. Luminance signal output

   An emitter follower provides a low impedance output signal of 3 V black-to-white amplitude at nominal contrast setting having a black level in the range 0 to +3 V. An external emitter load resistor is required, not less than 1 kΩ.
   Black level shift at contrast control is max. ± 20 mV if the luminance input current during black level is about 0,75 mA. When this current has a different value larger black level shift has to be taken into account. If the input current during black level differs 1 mA from the nominal value of 0,75 mA, the black level shift will be about 100 mV over the complete contrast control range. For smaller differences of the input current the black level shift will be correspondingly smaller.
   Black level shift with video signal content occurs only when the input signal is a.c.

APPLICATION INFORMATION (continued)

coupled. The value depends on the drive current amplitude and can be calculated from the figures given above (for maximum contrast; for a lower contrast setting the variation is correspondingly smaller).
Black level shift over an ambient temperature variation of 30 °C is typ. −140 mV.

6. The d.c. level of the luminance output signal may be controlled by the d.c. potential applied to this pin

Over the range of potential +0,9 to +1,7 V the black level of the luminance output signal (pin 5) is increased from 0 to +2,7 V. The output signal black level remains at +2,7 V when the potential on pin 6 is increased above +1,7 V.

7. Burst output

A 1 V peak-to-peak burst (kept constant by the a.c.c. system) is produced here. Also, to achieve good d.c. stability by negative feedback in the burst channel the d.c. potential at this pin is fed back to pins 1 and 15 via the chroma input transformer. When limiting occurs the burst amplitude is min. 2,5 V.

8. Fly-back blanking input waveform

Negative-going horizontal and vertical blanking pulses may be applied here. If rectangular blanking pulses of not greater than −1 V negative excursion are applied the signal level at the luminance output (pin 5) during blanking will be 0 V. However, if the blanking pulses applied to pin 8 have an amplitude of −2 to −3 V the signal level at the luminance output during blanking will be +1,5 V.

9. Chroma signal output

With an 1 V peak-to-peak burst output signal (pin 7) and at nominal contrast and saturation setting (pins 2 and 13) the chroma signal output amplitude is 2 V peak-to-peak. An external d.c. network is required which provides negative feedback in the chroma channel via pin 12.

10. Burst gating and clamping pulse input

A positive pulse of minimum 50 μA is required on this pin to provide gating in the burst channel and luminance channel black-level clamp circuit. The timing and width of this current pulse should be such that no appreciable encroachment occurs into the sync pulse or picture line periods during normal operation of the receiver.

11. +12 V power supply

Correct operation occurs within the range 10 to 13 V. All signal and control levels have a linear dependency on supply voltage but, in any given receiver design this range may be restricted due to considerations of tracking between the power supply variations and picture contrast and chroma levels. The power dissipation must not exceed 550 mW at 60 °C ambient temperature.

12. D.C. feedback for chroma channel (see pin 9)

APPLICATION INFORMATION (continued)

13. Chroma saturation control

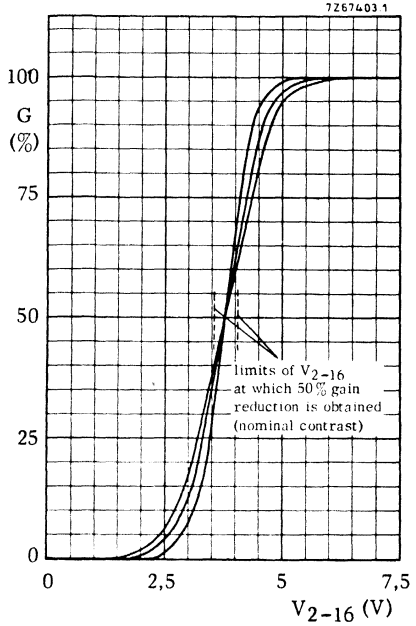
    A control range of +6 to > +14 dB is provided over a range of d.c. potential on pin 13 from +2,7 to +6,2 V. Colour killing is also done at this terminal by reducing the d.c. potential to less than +1 V, e.g., from the TBA540 colour killer output terminal. The kill factor is min. 40 dB.

14. A.C.C. input

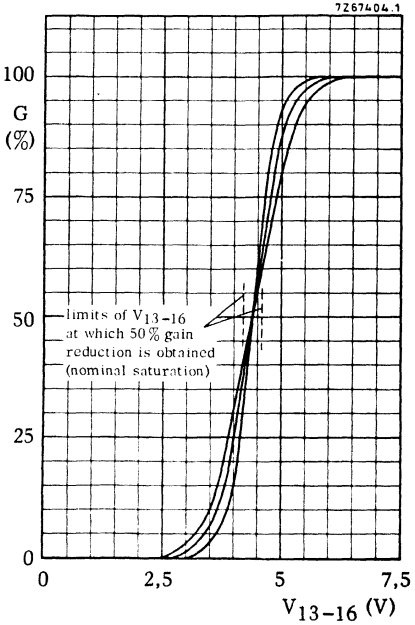
    A negative-going potential gives a 26 dB range of a.c.c. starting at +1,2 V and giving maximum gain reduction at an input voltage of min. 500 mV.

15. Chroma signal input (see pin 1)

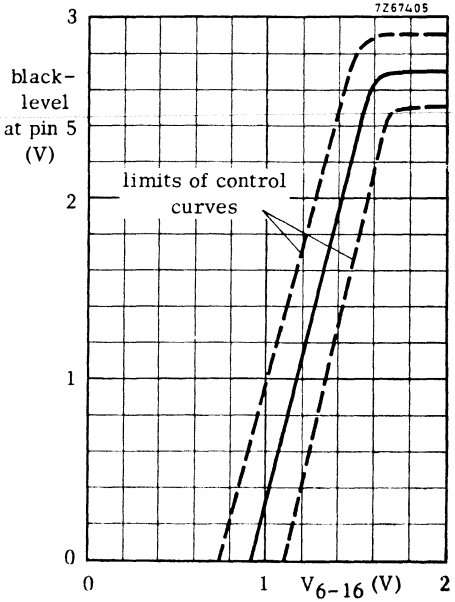
16. Negative supply (earth)



Contrast control of luminance amplifier



Saturation of chrominance amplifier



Control of black level at output luminance amplifier

LUMINANCE AND CHROMINANCE CONTROL COMBINATION

The TBA560C is a monolithic integrated circuit used in the decoding system of colour television receivers. The circuit consists of a luminance and a chrominance amplifier.
The luminance amplifier input is matched to the luminance delay line and performs the following functions:
d.c. contrast control * brightness control * black level clamping * blanking.

The chrominance amplifier comprises:
gain-controlled amplifier * chrominance gain control tracked with contrast control * separate d.c. saturation control * P. A. L. delay line driver * burst gate * colour killer.
Compared with the TBA560B the TBA560C produces a higher gain of the burst signal and consequently a smaller ratio of the chrominance output signal to the burst output signal.

QUICK REFERENCE DATA

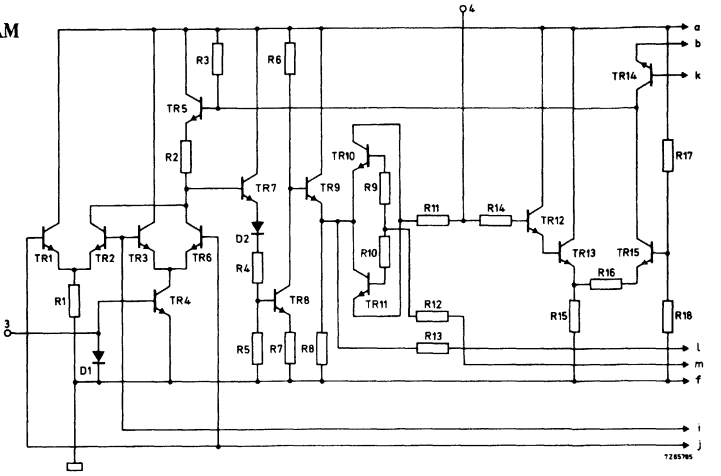
Supply voltage	V_{11-16}	nom.	12	V	
Supply current	I_{11}	nom.	30	mA	
Luminance signal input current	$I_{3(p-p)}$	typ.	1,5	mA	
Chrominance input signal	$V_{1-15(p-p)}$	$\geq$	4	mV	
		$<$	80	mV	
Luminance output signal at nominal contrast setting	$V_{5-16(p-p)}$	typ.	3	V	[1]
Chrominance output signal at nominal contrast and saturation setting	$V_{9-16(p-p)}$	typ.	1	V	[1]
Contrast control range		$\geq$	20	dB	
Saturation control range		$\geq$	20	dB	
Burst output (closed a.c.c. loop)	$V_{7-16(p-p)}$	typ.	1	V	

[1]) Nominal setting: maximum contrast and/or saturation minus 6 dB

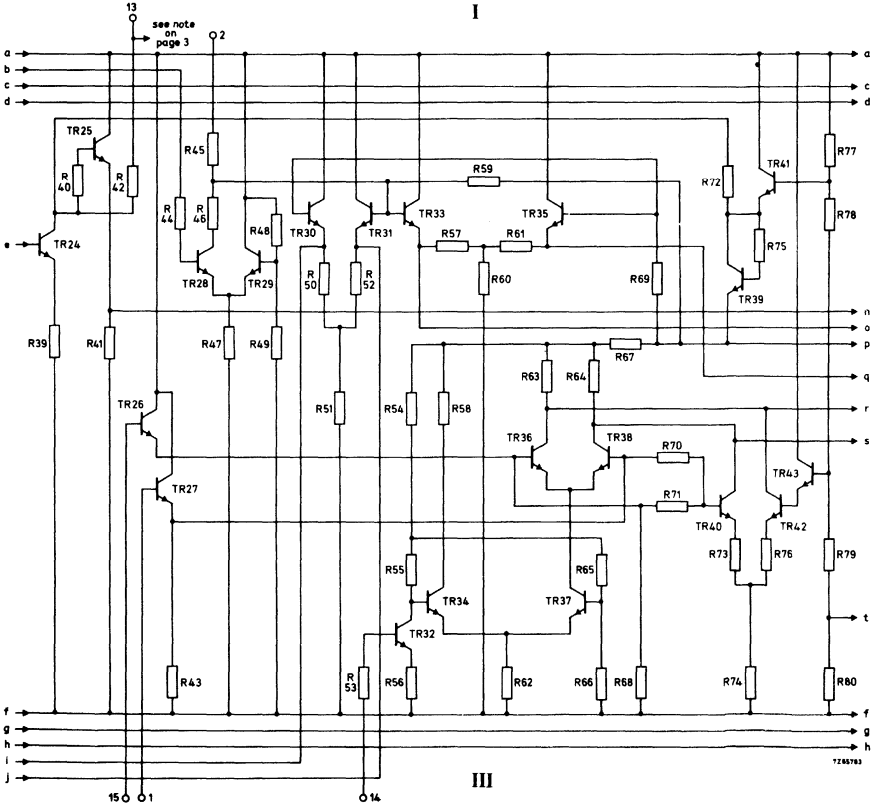
PACKAGE OUTLINE

TBA560C : 16-lead plastic dual in-line (type A) (See General Section)
TBA560CQ: 16 lead plastic quadruple in-line (See General Section)

CIRCUIT DIAGRAM

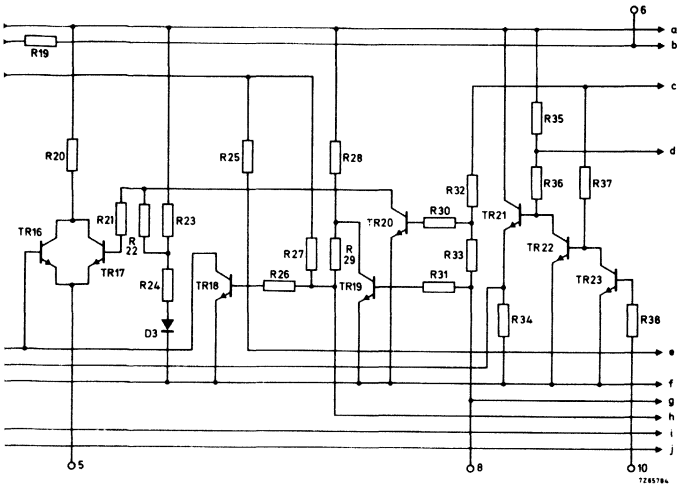


I



III

Note: the circuits are interconnected in the numerical sequence I, II, III, IV


R19
R20
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R28
R35
R36
R37
R32
R30
R33
R31
R34
R38
R21
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R23
R24
R26
R27
R29
TR16
TR17
TR18
TR19
TR20
TR21
TR22
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i
j
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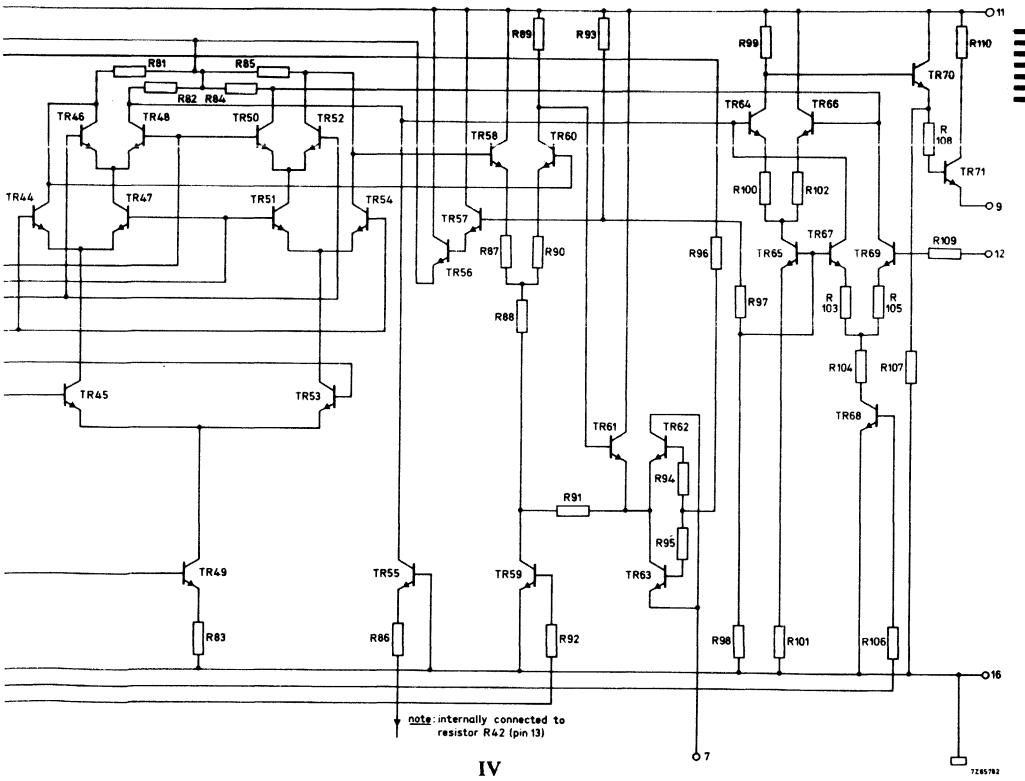
10
6
7Z65784

II


R81
R85
R82
R84
R89
R93
R99
R110
TR46
TR48
TR50
TR52
TR58
TR60
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R107
TR68
TR61
TR62
R94
R91
R95
TR49
TR55
TR59
TR63
R83
R86
R92
R98
R101
R106
note: internally connected to resistor R42 (pin 13)
11
9
12
16
7
7Z65782

IV

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage	V_{11-16}	max.	13	V [1]

Power dissipation

Total power dissipation	P_{tot}	max.	510	mW [1]

Temperatures

Storage temperature	T_{stg}	−25 to +125	°C
Operating ambient temperature	T_{amb}	0 to +60	°C

Voltages with respect to pin 16

V_{1-16}	0 to +5 V	V_{10-16}	min. −5 V
V_{2-16}	0 to +12 V [2]	V_{12-16}	−5 to +6 V
V_{4-16}	0 to +6 V	V_{13-16}	−3 to +6,5 V [2]
V_{6-16}	0 to +3 V	V_{14-16}	min. −5 V
V_{8-16}	−5 to +5 V	V_{15-16}	0 to +5 V

Currents (positive when flowing into the integrated circuit)

I_1	0 to +1 mA	I_7	−3 to +2 mA
I_3	−1 to +3 mA	I_9	−10 to 0 mA
I_5	−5 to 0 mA	I_{10}	max. +3 mA
I_6	−1 to +1 mA	I_{14}	max. +1 mA
		I_{15}	0 to +1 mA

[1] Permissible while tubes are heating up: V_{11-16} max. 16 V and P_{tot} max. 700 mW.

[2] V_{2-16} and V_{13-16} must always be lower than V_{11-16}.

CHARACTERISTICS measured in the circuit on page 6

Supply voltage	V_{11-16}	typ.	12	V	
			10 to 13	V	
Required input signals at V_{11-16} = 12 V and T_{amb} = 25 °C					
Chrominance input signal					
peak-to-peak value	$V_{1-15(p-p)}$		4 to 80	mV	
Luminance input current					
black-to-white value	I_3	typ.	1,5	mA	
Contrast control voltage range					
for 20 dB of control	V_{2-16}	see graph on page 11			
Brightness control voltage	V_{6-16}	see graph on page 11			[1]
Saturation control voltage range					
for 20 dB of control	V_{13-16}	see graph on page 11			
Burst keying pulse (positive)					
peak-to-peak value	$I_{10(p-p)}$		0,05 to 1	mA	
Fly-back blanking pulses (negative)					
peak-to-peak value					
for 0 V blanking level at pin 5	$V_{8-16(p-p)}$	typ.	−0,5	V	
for 1,5 V blanking level at pin 5	$V_{8-16(p-p)}$	typ.	−2,5	V	
Colour killer	V_{13-16}	<	1	V	
Automatic chrominance control starting	V_{14-16}	typ.	1,2	V	[2]

[1] When V_{6-16} is increased above 1,7 V the black level of the output signal remains at 2,7 V

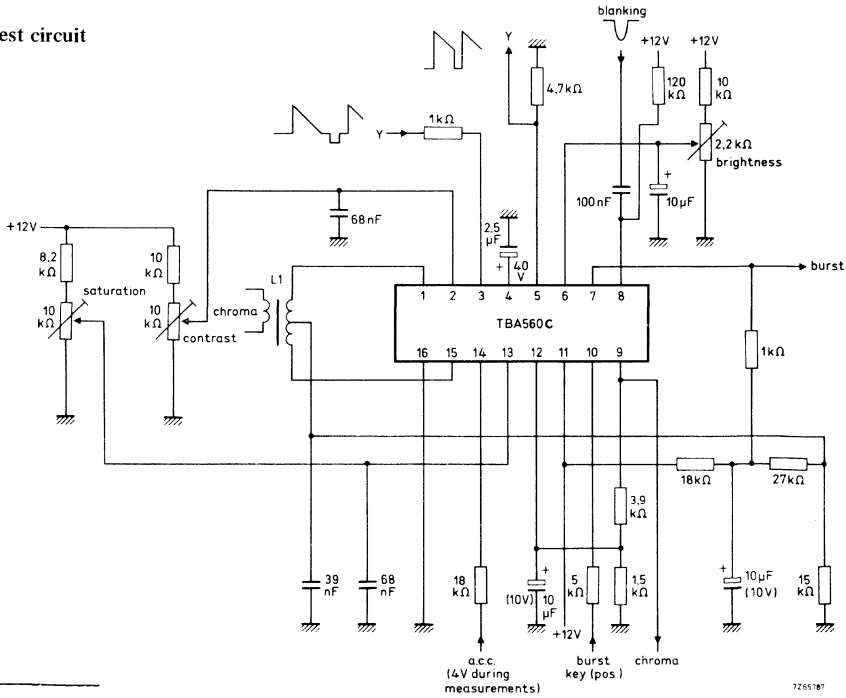
[2] A negative going potential provides a 26 dB a.c.c. range with negligible signal distortion. Maximum gain reduction is obtained at an input voltage of min. 500 mV.

CHARACTERISTICS (continued)

Obtainable output signals

Luminance output voltage at nominal contrast (peak-to-peak value)	$V_{5-16(p-p)}$	typ.	3	V	[1]
Burst signal (peak-to-peak value)	$V_{7-16(p-p)}$	typ.	1	V	[2]
Chrominance signal at nominal contrast and saturation (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	1	V	[1]
3 dB bandwidth of chrominance and luminance amplifier	B	typ.	5	MHz	
Change of ratio luminance to chrominance signals at 10 dB contrast control		<	2	dB	

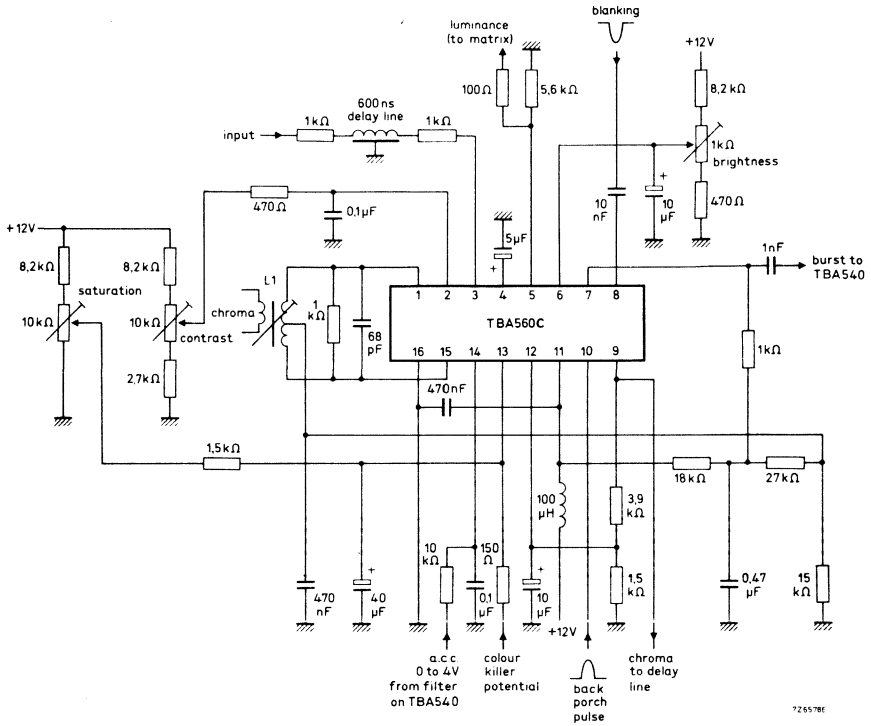
Test circuit



[1]) Nominal setting: maximum contrast and/or saturation minus 6 dB.

[2]) Burst signal is kept constant at 1 V peak-to-peak by automatic gain control.

APPLICATION INFORMATION



Application diagram for operation in combination with the TBA540.

APPLICATION INFORMATION (continued)

Pinning

1. Balanced chroma signal input
2. Contrast control
3. Luminance signal input
4. Black level clamp capacitor
5. Luminance signal output
6. Brightness control
7. Burst output
8. Fly-back blanking input
9. Chroma signal output
10. Burst gate and clamping pulse input
11. Supply voltage (12 V)
12. D.C. feedback for chroma channel
13. Chroma saturation control
14. A.C.C. input
15. Chroma signal input
16. Earth (negative supply)

The function is quoted against the corresponding pin number

1. Balanced chroma signal input (in conjunction with pin 15)

   This is derived from the chroma signal bandpass filter, designed to provide the push-pull input. An input signal amplitude of at least 4 mV peak-to-peak is required on pins 1 and 15. Both pins require a d.c. potential of approximately +3,0 V. This is derived as a common-mode signal from a network connected to pin 7 (burst output). In this way d.c. feedback is provided over the burst channel to stabilise its operation.
   All figures for the chrominance signals are based on a colour bar signal with 75% saturation: i.e. burst-to-chroma ratio of input signal is 1 : 2.

2. D.C. contrast control

   With +3,7 V on this pin, the gain in the luminance channel is such that a 1,5 mA peak-to-peak input signal to pin 3 gives a luminance output signal amplitude on pin 5 of 3 V black-to-white. A variation of voltage on pin 2 between +6 V and +2 V gives a corresponding gain variation of +6 to > −14 dB. A similar variation in gain in the chroma channel occurs in order to provide the correct tracking between the two signals.

3. Luminance signal input

   This terminal has a very low input impedance and acts as a current sink. The luminance signal from the delay line is fed via a series terminating resistor and must have about 1,5 mA black-to-white amplitude.

4. Charge storage capacitor for black level clamp (5,0 μF)

5. Luminance signal output

   An emitter follower provides a low impedance output signal of 3 V black-to-white amplitude at nominal contrast setting having a black level in the range 0 to +3 V. An external emitter load resistor is required, not less than 1 kΩ.
   Black level shift at contrast control is max. ± 20 mV if the luminance input current during black level is about 0,75 mA. When this current has a different value a larger black level shift has to be taken into account. If the input current during black level differs 1 mA from the nominal value of 0,75 mA, the black level shift will be about 100 mV over the complete contrast control range. For smaller differences of the input current the black level shift will be correspondingly smaller.
   Black level shift with video signal content occurs only when the input signal is a.c. coupled. The value depends on the drive current amplitude and can be calculated from

APPLICATION INFORMATION (continued)

the figures given above (for maximum contrast; for a lower contrast setting the variation is correspondingly smaller).
Black level shift over an ambient temperature variation of 30 °C is typ. −140 mV.

6. The d.c. level of the luminance output signal may be controlled by the d.c. potential applied to this pin

Over the range of potential +0,9 to +1,7 V the black level of the luminance output signal (pin 5) is increased from 0 to +2,7 V. The output signal black level remains at +2,7 V when the potential on pin 6 is increased above +1,7 V.

7. Burst output

A 1 V peak-to-peak burst (kept constant by the a.c.c. system) is produced here. Also, to achieve good d.c. stability by negative feedback in the burst channel the d.c. potential at this pin is fed back to pins 1 and 15 via the chroma input transformer. When limiting occurs the burst amplitude is min. 2,5 V.

8. Fly-back blanking input waveform

Negative-going horizontal and vertical blanking pulses may be applied here. If rectangular blanking pulses of not greater than −1 V negative excursion are applied the signal level at the luminance output (pin 5) during blanking will be 0 V. However, if the blanking pulses applied to pin 8 have an amplitude of −2 to −3 V the signal level at the luminance output during blanking will be +1,5 V.

9. Chroma signal output

With an 1 V peak-to-peak burst output signal (pin 7) and at nominal contrast and saturation setting (pins 2 and 13) the chroma signal output amplitude is 1 V peak-to-peak. An external d.c. network is required which provides negative feedback in the chroma channel via pin 12.

10. Burst gating and clamping pulse input

A positive pulse of minimum 50 μA is required on this pin to provide gating in the burst channel and luminance channel black-level clamp circuit. The timing and width of this current pulse should be such that no appreciable encroachment occurs into the sync pulse or picture line periods during normal operation of the receiver.

11. +12 V L.T power supply

Correct operation occurs within the range 10 to 13 V. All signal and control levels have a linear dependency on supply voltage but, in any given receiver design this range may be restricted due to considerations of tracking between the power supply variations and picture contrast and chroma levels. The power dissipation must not exceed 550 mW at 60 °C ambient temperature.

12. D.C. feedback for chroma channel (see pin 9)

13. Chroma saturation control

A control range of +6 to > +14 dB is provided over a range of d.c. potential on pin 13 from +2,7 to +6,2 V. Colour killing is also done at this terminal by reducing the d.c. potential to less than +1 V, e.g., from the TBA540 colour killer output terminal. The kill factor is min. 40 dB.

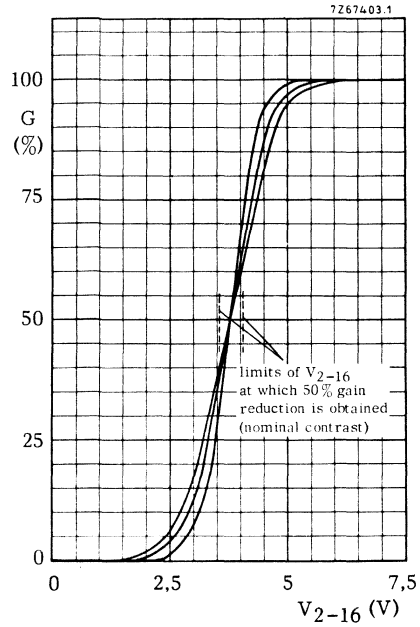
APPLICATION INFORMATION (continued)

14. A.C.C. input

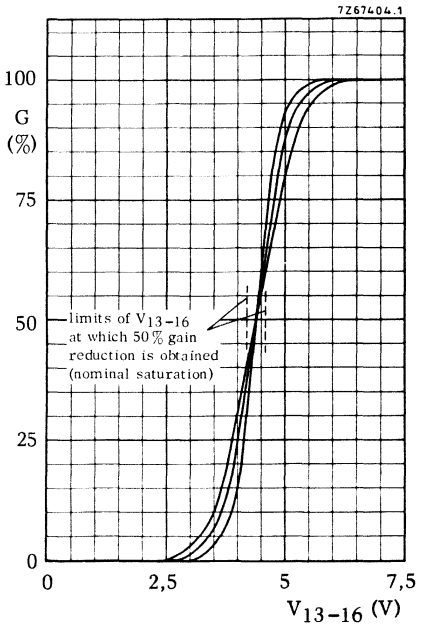
    A negative-going potential gives a 26 dB range of a.c.c. starting at +1, 2 V and giving maximum gain reduction at an input voltage of min. 500 mV.

15. Chroma signal input (see pin 1)

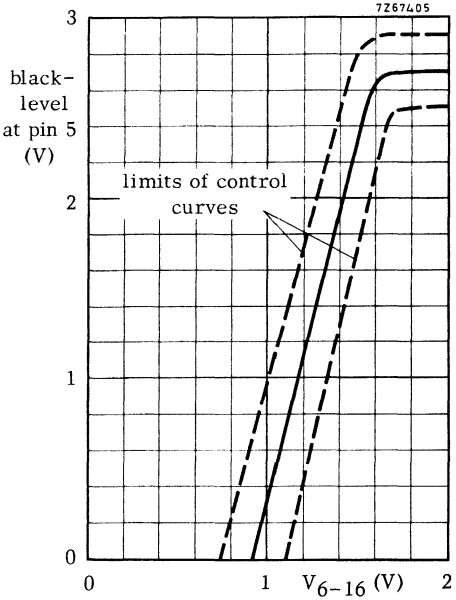
16. Negative supply (earth)



Contrast control of luminance amplifier



Saturation of chrominance amplifier



Control of black level at output luminance amplifier

INTEGRATED A.M./F.M. RADIO RECEIVER CIRCUIT

The TBA570 is a monolithic integrated circuit for use in a.m. (including the short-wave band), a.m./f.m. receivers.
Besides an audio preamplifier and driver, it incorporates signal detector, i.f. amplifier, mixer, local oscillator and a.g.c. for a.m.; limiter, complete i.f. amplifier, and stabilization circuit for the front-end base bias for f.m.
It is adapted to operate in conjunction with hybrid i.f. block filters and it can be fitted with a tuning indicator.
The TBA570 can drive output stages up to 3 W (AC187/AC188) or 5 W (AD161/AD162). [1])
It can also be used in complete tuner kits; the 500 mV a.f. output satisfies DIN standard 45 500.

QUICK REFERENCE DATA			
Applicable supply voltage range of receiver			3,6 V to 18 V[1])
Ambient temperature	T_{amb}		25 °C
Supply voltage	Vp	nom.	6 V
Total quiescent current (except output stages, driver stage TR31 and f.m. front end; V_P = 6 V)	I_{tot}	typ.	10,5 mA
A.F. output power at d_{tot} = 10 %, R_L = 4 Ω (with AC187/AC188 in portable receiver)	P_o	typ.	1 W
A.M. performance (at pin 2)			
R.F. input voltage (S/N = 26 dB)	V_i	typ.	18 μV
A.G.C. range (change of r.f. input voltage for 10 dB expansion in audio range)		typ.	65 dB
R.F. signal handling (d_{tot} = 10 %; m = 0,8)		typ.	150 mV
F.M. performance (at pin 2)			
R.F. input voltage 3 dB before limiting	V_i	typ.	80 μV

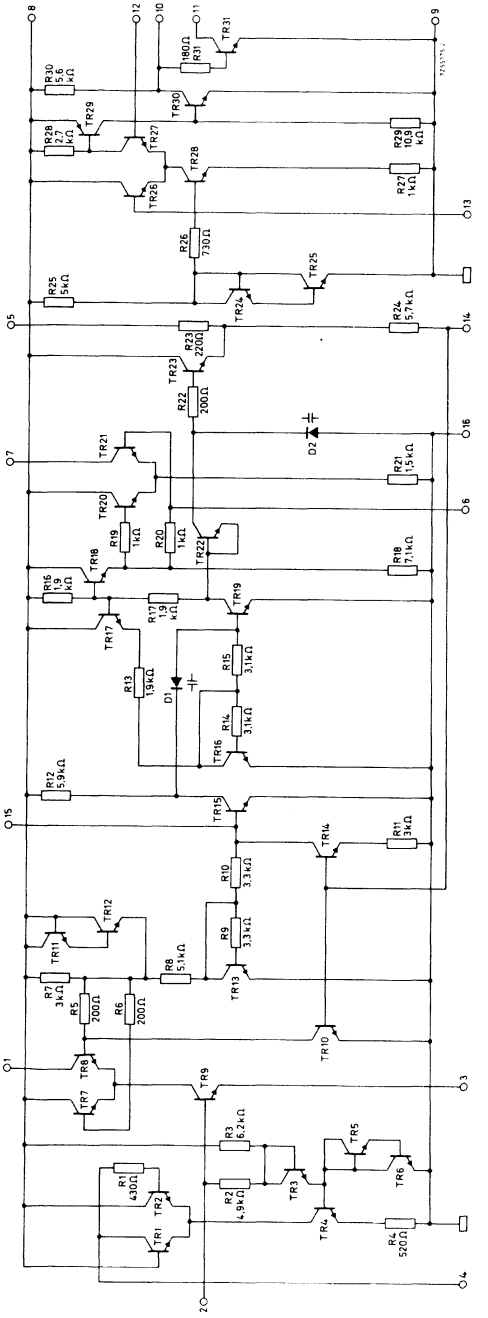
PACKAGE OUTLINE

TBA570 : 16 lead plastic dual in-line (type A) (See General Section)

TBA570Q: 16 lead plastic quadruple in-line (See General Section)

[1]) The data given in these sheets are based on a 6 V receiver with a 1 W output in which the voltage swing at pin 11 (a.f. driver) was 5,5 V; however, a maximum voltage swing V_{11-9} of 18 V is allowable, being required for mains and car-radio applications.

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Voltages

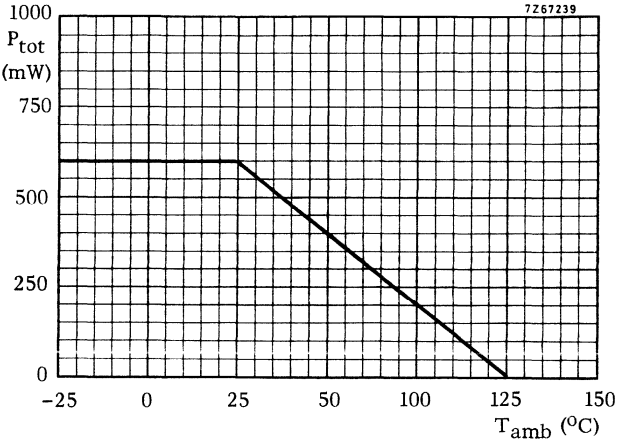
Pin No. 11 voltage	$V_{11\text{-}9}$	max.	18	V
Pin No. 8 voltage	$V_{8\text{-}16}$	max.	8	V

Current

Pin No. 11 current (peak value)	I_{11M}	max.	50	mA

Dissipation

Total power dissipation — See derating curve below



Temperatures

Storage temperature	T_{stg}	−55 to +125	°C
Operating ambient temperature (see also derating curve above)	T_{amb}	−20 to +125	°C

DESIGN DATA

Pins not under measuring condition should not be connected.

Voltages with respect to pins 9 and 16 (tolerated minimum: 0 V)

Pins No. 1 and 7 voltage	$V_{1\text{-}9(16)}$; $V_{7\text{-}9(16)}$	max.	18 V
Pin No. 4 voltage	$V_{4\text{-}9(16)}$	max.	8 V
Pin No. 8 voltage	$V_{8\text{-}9(16)}$	max.	8 V
Pin No. 3 voltage	$V_{3\text{-}9(16)}$	max.	3 V
Pin No. 5 voltage	$V_{5\text{-}9(16)}$	max.	4 V
Pin No. 14 voltage	$V_{14\text{-}9(16)}$	max.	1 V

Currents (tolerated minimum: 0 mA)

Pins No. 2, 6, 12, 13, 15 current	$I_2;I_6;I_{12}$; $I_{13};I_{15}$	max.	80 μA
Pin No. 10 current	I_{10}	max.	5 mA

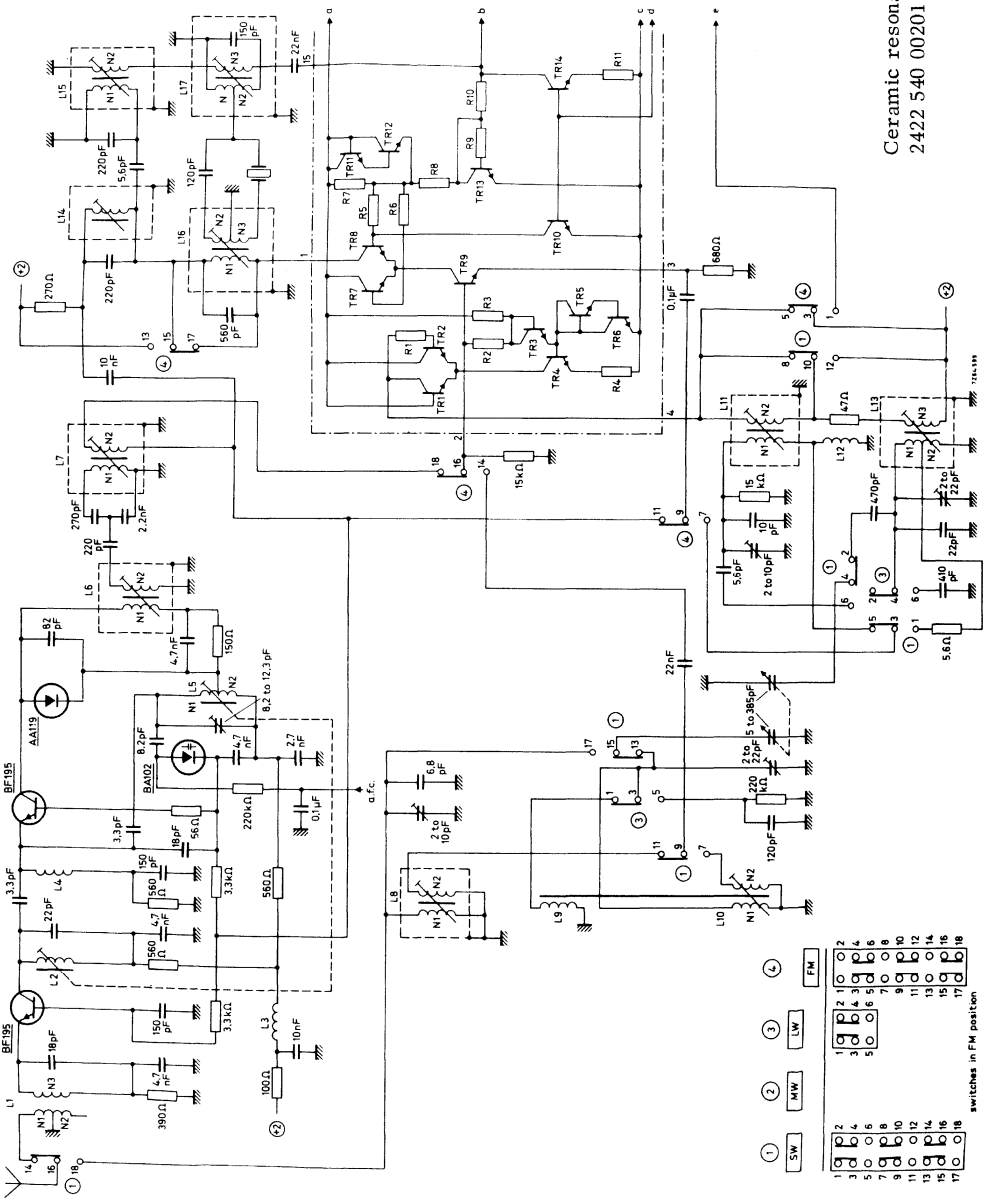
D.C. CHARACTERISTICS at T_{amb} = 25 °C

Saturation voltage of TR31 at I_C = 50 mA; I_B = 2,5 mA	V_{CEsat}	<	1,0 V
Collector breakdown voltage of TR31 (pin 11) at I_C = 25 mA; R_{BE} = 7 kΩ	V_{CER}	>	18 V
D.C. current gain of driver stage TR31 at I_C = 50 mA	h_{FE}	>	25
Total quiescent current except TR31 collector current, f.m. front-end and discrete output stages; V_P = 6 V	I_{tot}	typ.	10,5 mA
V_P = 9 V	I_{tot}	typ.	14,0 mA
Total power dissipation at pin 8 (excluding TR31) at V_P = 9 V; V_{8-16} = 7,8 V	$P_{tot(8)}$	typ.	100 mW
Applicable supply voltage range of receiver	V_P		3,6 to 18 V[1])
Base bias voltage for f.m. front-end at a total external load current at pin 2 of $-I_2$ = 150 μA	V_{2-16}	typ.	1,2 V

A.C. CHARACTERISTICS at T_{amb} = 25 °C; V_P = 6 V ; I_E (TR9) = 1 mA

			450 kHz	1 MHz	10,7 MHz
Input conductance at pin 2	g_{ie}	typ.	–	0,4	0,5 mA/V
Output conductance at pin 1	g_{oe}	typ.	6	–	90 μA/V
Input conductance at pin 15	g_{ie}	typ.	0,35	–	0,7 mA/V

[1]) See max. tolerated voltages for pins 1, 4, 7, 8 and 11 in design data on page 4.


Ceramic resonator:
2422 540 00201
switches in FM position
SW
MW
LW
FM

COIL DATA

1. A.M. – I.F. coils (f_o = 455 kHz)

I. F. bandpass filter

L16: N_1 = 221, 4 µH
Q_o = 128
N_1/N_2 = 20
N_2/N_3 = 1, 2
$|Z_T|$ = 2, 8 kΩ

L17: N_1 = 827 µH
Q_o = 136
N_2/N_1 = 36
$N_2 + N_1/N_3$ = 22, 4

2. F.M. – I.F. coils

(f_o = 10, 7 MHz)

First i.f. bandpass filter

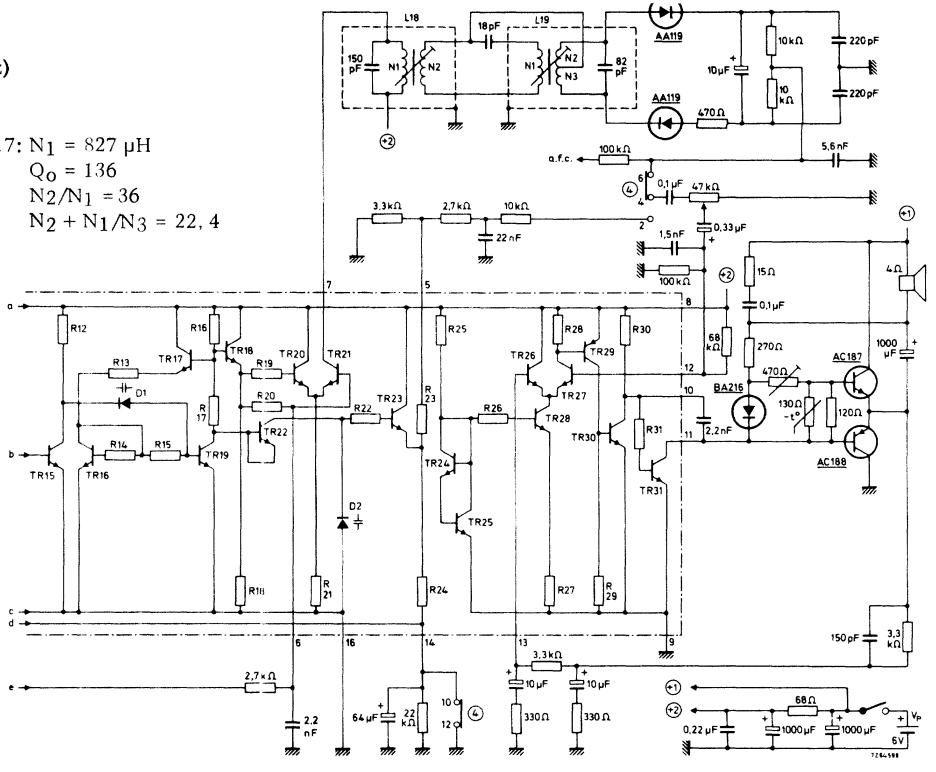
L6: N_1 = 2, 7 µH
Q_o = 90
$kQ_{L6\text{-}L7}$ = 1, 2
N_1/N_2 = 10

L7: N_1 = 1 µH
Q_o = 100
N_1/N_2 = 4, 5

Second i.f. bandpass filter

L14: N_1 = 1 µH
Q_o = 100
$kQ_{L14\text{-}L15}$ = 1, 2

L15: N_1 = 1 µH
Q_o = 100
N_1/N_2 = 3



Ratio detector

L18: N_1 = 1, 5 µH
Q_o = 95
$kQ_{L18\text{-}L19}$ = 0, 7
N_1/N_2 = 2

L19: $N_2 + N_3$ = 2, 7 µH
Q_o = 110
$N_2 + N_3/N_1$ = 5, 3
$N_2 = N_3$

APPLICATION INFORMATION (continued) at T_{amb} = 25 °C; V_P = 6 V.

See also circuit diagram on pages 6 and 7.

A.M. performance

R.F. input voltage for signal to noise ratio of 26 dB	V_i	typ.	18 μV [1) 2)]
R.F. input voltage for 10 mV (a.f.) across volume control	V_i	typ.	4 μV [1) 2)]
A.F. voltage across volume control at 100 μV (r.f.) input voltage	V_o	typ.	80 mV [1) 2)]
Signal to noise ratio at 1 mV (r.f.) input voltage	S/N	typ.	50 dB [1) 2)]
A.G.C. range (change in r.f. input voltage for 10 dB expansion in audio range)		typ.	60 dB [1) 2)]
R.F. signal handling capability at 80 % modulation (d_{tot} < 10 %)	V_i	typ.	150 mV [1)]
Harmonic distortion of h.f. part (over most of a.g.c. range; m = 0,3; f_m = 1 kHz)	d_{tot}	typ.	1 %
I.F. selectivity	S_9	typ.	33 dB
I.F. bandwidth	B_{3dB}	typ.	5 kHz

1) a. A.F. signal: measured across volume control.
b. R.F. signal: measured at pin 2 with the antenna circuit connected (source resistance of about 1 kΩ).
c. f_o = 1 MHz; f_m = 1 kHz.

2) m = 0,3.

APPLICATION INFORMATION (continued) at T_{amb} = 25 °C; V_P = 6 V.

See also circuit diagram on pages 6 and 7.

F.M. performance

Sensitivity for an f.m. signal, 3dB before limiting			
at 75 Ω aerial input of f.m. front end	V_i	typ. 6,5 μV	1)
at pin 2 (first i.f.)	V_i	typ. 80 μV	2)
Sensitivity for 26 dB S/N ratio at 75 Ω aerial input of f.m. front end	V_i	typ. 4 μV	1)
A.F. output voltage across volume control at an i.f. signal beyond limiting	V_o	typ. 75 mV	2)
S/N ratio over most of signal range	S/N	typ. 55 dB	2)
A.M. suppression over most of signal range		> 45 dB	2) 3)
I.F. selectivity	S_{300}	typ. 43 dB	4)
I.F. bandwidth	B_{3dB}	typ. 170 kHz	4)
A.F. signal distortion, 3 dB before i.f. limiting	d_{tot}	typ. 1 %	5)

Audio performance

A.F. output power at d_{tot} = 10 %	P_o	typ. 1 W	6)
at onset of clipping	P_o	typ. 800 mW	6)
Distortion before clipping	d_{tot}	typ. 0,5 %	6)
A.F. input signal (at pin 12)			
at P_o = 50 mW	V_i	typ. 4 mV	6)
at P_o = 800 mW	V_i	typ. 15 mV	6)
Noise output power (volume control at minimum)	P_N	typ. 20 nW	7)
Typical overall fidelity (flat within 3 dB)		60 Hz to 15 kHz	
Open loop voltage gain	G_v	typ. 95 dB	

1) Aerial e.m.f. (V_i) at f_o = 100 MHz; R_S = 75 Ω (source impedance; see page 11). Δf = ±15 kHz; f_m = 1 kHz.

2) f_o = 10,7 MHz; Δf = ±15 kHz; f_m = 1 kHz.

3) A.M. signal; m = 0,3; f_m = 400 Hz. (carrier simultaneously modulated with a.m. and f.m.)

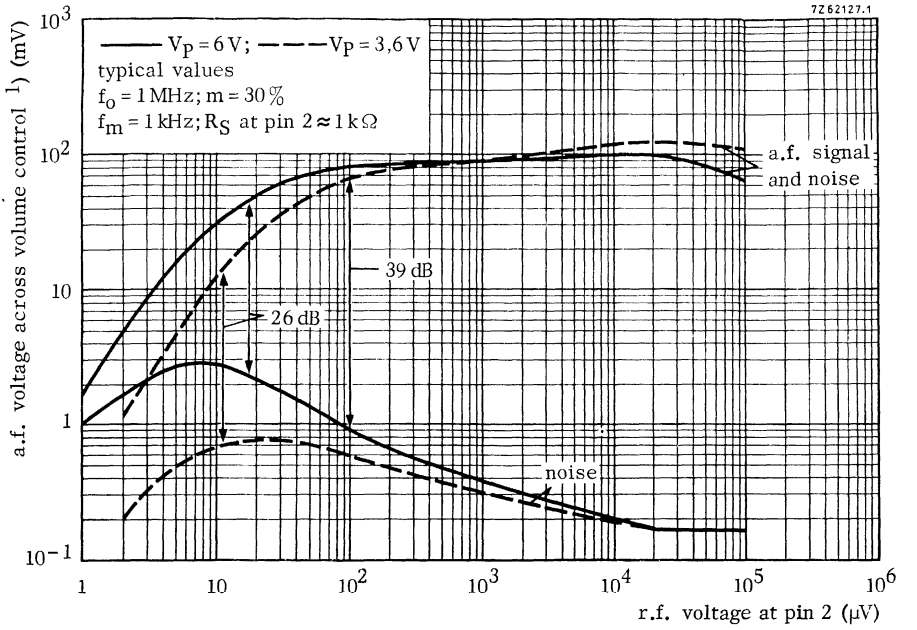
4) Including ratio detector.

5) f_o = 100 MHz; Δf = ±40 kHz; f_m = 1 kHz.

6) Measured at 1 kHz, a negative feedback of 55 dB and a loudspeaker of 4 Ω.

7) Measured at a bandwidth of 60 Hz to 15 kHz, pin 12 being connected via a capacitor of 32 μF to pin 9; loudspeaker impedance 4 Ω.

APPLICATION INFORMATION (continued) at T_{amb} = 25 °C; V_P = 6 V

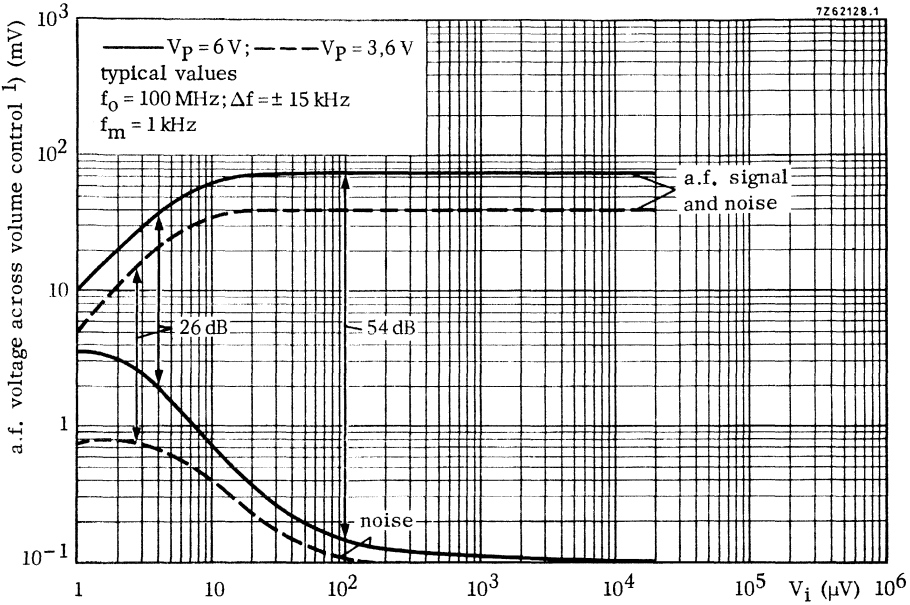


Typical a.g.c. curves at a.m. reception

A.F. voltage across volume control versus r.f. voltage at pin 2.

[1]) Slider at lower end.

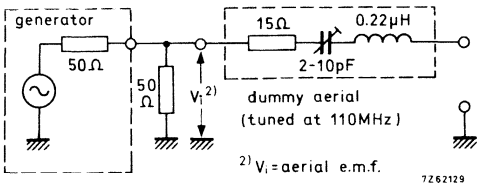
APPLICATION INFORMATION (continued)



Typical S/N curves at f.m. reception.

A.F. voltage across volume control versus aerial e.m.f. of a dummy aerial connected to the 75 Ω input of the f.m. front-end.

Test circuit



[1]) Slider at lower end

RING (DE)MODULATOR FOR TELEPHONY AND INDUSTRIAL EQUIPMENT

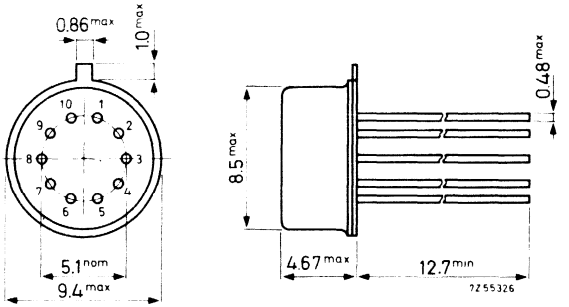
The TBA673 is a monolithic integrated circuit comprising a 4-transistor modulator and demodulator circuit. This device is a high voltage version of the TAB101.
The four transistors must be as identical as possible; the lay-out has been designed to achieve this and the best possible tracking of the transistor parameters with temperature.

QUICK REFERENCE DATA				
Collector cut-off current $I_E = 0$; $V_{CB} = 5$ V; $T_{amb} = 25\ ^oC$	I_{CBO}	<	100	nA
Base-emitter voltage differences between transistors 1, 2, 3, 4 $V_{CB} = 5$ V; $-I_E = 150\ \mu A$	$\lvert V_{BE1} - V_{BE2} \rvert$	<	5	mV
	$\lvert V_{BE3} - V_{BE4} \rvert$	<	5	mV
D.C. current gain differences between transistors 1, 2, 3, 4 $V_{CB} = 5$ V; $-I_E = 150\ \mu A$	$\lvert h_{FB1} - h_{FB2} \rvert$	<	0,008	
	$\lvert h_{FB3} - h_{FB4} \rvert$	<	0,008	

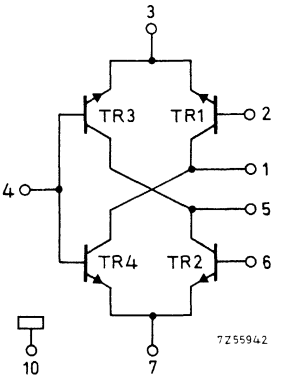
PACKAGE OUTLINE

Dimensions in mm

TO-74 (reduced height)



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages (each transistor)

Collector-emitter voltage (open base)	V_{CEO}	max.	17,5	V
Emitter-base voltage (open collector)	V_{EBO}	max.	6,2	V
Collector-substrate voltage	V_{CS}	max.	65	V

Currents (each transistor)

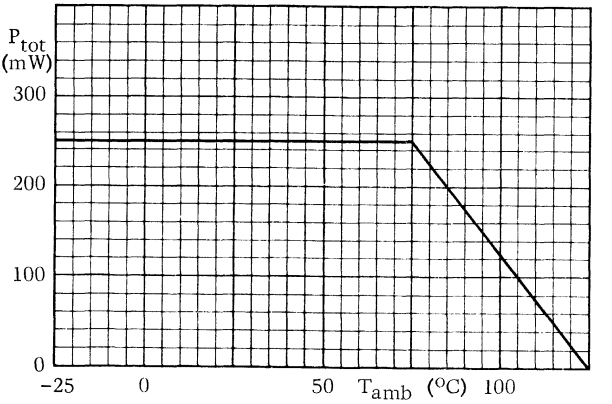
Collector current	I_C	max.	20	mA

Power disspation (4 transistors)

Total power dissipation — See curve below

Temperatures

Storage temperature	T_{stg}	−55 to +125	°C
Operating ambient temperature	See curve below		

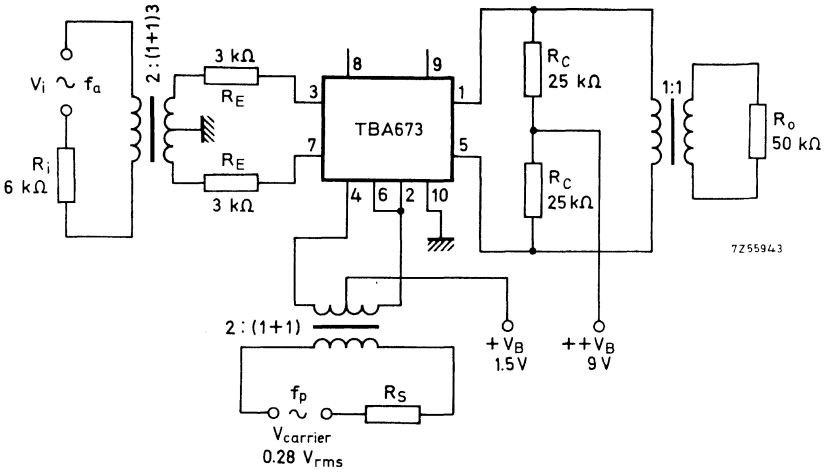


CHARACTERISTICS T_{amb} = 25 °C unless otherwise specified

Collector cut-off current				
I_E = 0; V_{CB} = 5 V	I_{CBO}	typ. <	5 100	nA nA
Collector-substrate leakage current				
V_{CS} = 5 V	I_{CS}	typ. <	5 100	nA nA
Emitter cut-off current				
I_C = 0; V_{EB} = 1 V	I_{EBO}	typ. <	5 100	nA nA
Breakdown voltages				
I_E = 0; I_C = 50 µA	$V_{(BR)CBO}$	>	45	V
I_B = 0; I_C = 200 µA	$V_{(BR)CEO}$	>	17,5	V
$-I_S$ = 50 µA	$V_{(BR)CS}$	>	65	V
I_C = 0; I_E = 10 µA	$V_{(BR)EBO}$	>	6,2	V
D.C. current gain				
I_C = 150 µA; V_{CB} = 5 V	h_{FE}	> typ.	35 90	
I_C = 10 mA; V_{CB} = 5 V	h_{FE}	> typ.	35 75	
Transition frequency at f = 35 MHz				
I_C = 150 µA ; V_{CB} = 5 V	f_T	typ.	160	MHz
I_C = 1 mA ; V_{CB} = 5 V	f_T	typ.	300	MHz
Collector-base capacitance				
V_{CB} = 5 V; I_E = 0	C_{cb}	typ.	0,4	pF
Collector-substrate capacitance				
V_{CS} = 5 V; I_E = 0	C_{cs}	typ.	2,8	pF
Base-emitter voltage difference				
between transistors TR1 and TR2 at $-I_{E1} = -I_{E2}$ = 150 µA; $V_{CB1} = V_{CB2}$ = 5 V	$\lvert V_{BE1} - V_{BE2} \rvert$	typ. <	2 5	mV mV
between transistors TR3 and TR4 at $-I_{E3} = -I_{E4}$ = 150 µA; $V_{CB3} = V_{CB4}$ = 5 V	$\lvert V_{BE3} - V_{BE4} \rvert$	typ. <	2 5	mV mV
D.C. current gain differences				
between transistors TR1 and TR2 at $-I_{E1} = -I_{E2}$ = 150 µA; $V_{CB1} = V_{CB2}$ = 5 V	$\lvert h_{FB1} - h_{FB2} \rvert$	typ. <	0,002 0,008	
between transistors TR3 and TR4 at $-I_{E3} = -I_{E4}$ = 150 µA; $V_{CB3} = V_{CB4}$ = 5 V	$\lvert h_{FB3} - h_{FB4} \rvert$	typ. <	0,002 0,008	

APPLICATION INFORMATION

Telephony carriers ring modulator



Performance at T_{amb} = 25 °C

Conversion gain at f_a = 1 kHz V_i = 0, 4 V; f_p = 34 kHz	G_c	typ.	−0, 75	dB
Carrier leakage power in R_o at f_p = 34 kHz	P_{oc}	typ.	3	nW

INTEGRATED A.M./F.M. RADIO RECEIVER CIRCUIT

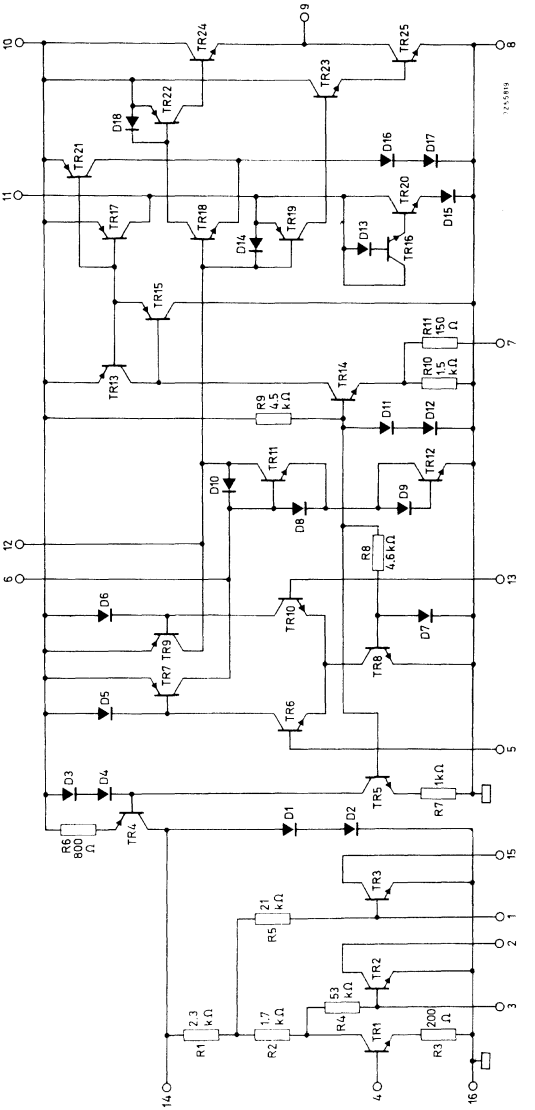
The TBA690 is a monolithic integrated circuit for use in a.m. (including the short-wave band), a.m./f.m. receivers.
It incorporates the class-B audio output stage (0,6 W), stabilization circuit for quiescent current, driver, pre-amplifier, 2-stage i.f. amplifier, a.g.c. and stabilized bias circuit.
The discrete input stage (for a.m.: mixer-oscillator; for f.m.: 1st i.f.) enables a high flexibility in circuit lay-out with conventional or lumped selectivity.
The internal stabilization ensures negligible loss of sensitivity and cross-over distortion over a wide supply voltage range from 2,7 V to 12 V.

QUICK REFERENCE DATA				
Applicable supply voltage range of receiver	V_{10-8}		2,7 to 12	V [1]
Ambient temperature	T_{amb}		25	°C
Supply voltage	V_P	nom.	6	V
Total quiescent current (inclusive discrete input transistor, exclusive f.m. front end)	I_{tot}	typ.	17	mA
A.F. output power at d_{tot} = 10 %, R_L = 4 Ω	P_o	typ.	600	mW
A.M. performance				
R.F. input voltage (S/N = 26 dB) (at base of external mixer-oscillator)	V_i	typ.	15	μV
A.G.C. range (change of r.f. input voltage for 10 dB expansion in audio range)		typ.	72	dB
F.M. performance				
R.F. input voltage (at base of external i.f. stage) 3 dB before limiting	V_i	typ.	100	μV

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) (See General Section)

[1]) The data given in this sheet are based on a receiver with V_P = 6 V; P_o = 600 mW.

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Pin No. 10 voltage	V_{10-8}	max.	12	V	
Pins No. 15, 9, 2 voltages	V_{15-8}, V_{9-8}, V_{2-8}	max.	11,4	V	
Pin No. 16 voltage	V_{16-8}	max.	0	V	1)
Pin No. 7 voltage	$\pm V_{7-8}$	max.	5	V	
Pins No. 4, 3, 1 voltages	$-V_{4-16}$, $-V_{3-16}$, $-V_{1-16}$	max.	5	V	
Pin No. 5 voltage	$\pm V_{5-13}$	max.	5	V	
Pin No. 10 voltage	V_{10-9}	max.	11,4	V	

Currents

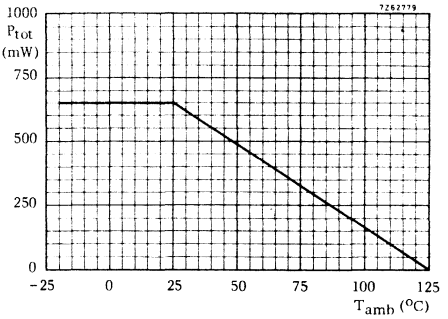
Pins No. 14, 12, 11, 6 currents	$I_{14}, I_{12}, I_{11}, I_6$	max.	5	mA	
Pins No. 13, 5, 4, 3, 1 currents	$I_{13}, I_5, I_4, I_3, I_1$	max.	0,5	mA	
Pins No. 15, 2 currents	I_{15}, I_2	max.	10	mA	
Pin No. 8 current	$-I_{8RM}$	max.	0,8	A	2)
Pin No. 9 current	$\pm I_{9RM}$	max.	0,8	A	2)
Pin No. 10 current	I_{10RM}	max.	0,8	A	2)

Dissipation

Total power dissipation				
at T_{amb} = 45 °C	P_{tot}	max.	520	mW
at T_{amb} = 25 °C	P_{tot}	max.	650	mW

Temperatures

Storage temperature	T_{stg}	−55 to +125	°C
Operating ambient temperature	T_{amb}	−20 to +125	°C



1) Substrate connected to pin 16.
2) Repetitive peak value; internally limited.

CHARACTERISTICS

D.C. characteristics at T_{amb} = 25 °C; V_P = 6 V

I.F. amplifier

Collector current of i.f. transistor TR2 (a.g.c. transistor "off")	I_C	typ. 0,55 to 1,6	1 	mA mA
Collector current of i.f. transistor TR3 (a.g.c. transistor "off")	I_C	typ. 1,4 to 4,2	2,5 	mA mA
Saturation voltage of i.f. transistor TR2 at $I_C \leq 2$ mA	V_{CEsat}	<	150	mV
Saturation voltage of i.f. transistor TR3 at $I_C \leq 5$ mA	V_{CEsat}	<	200	mV
Bias voltage for mixer and tuner	V_{14-16}	typ. 1,25 to 1,55	1,4 	V V
Temperature dependency of bias voltage V_{14-16}	T_c	typ.	-3,6	mV/°C
Bias current (available)	$-I_{14}$	<	100	µA

A.F. amplifier

Input common mode voltage range	V_{5-8}, V_{13-8}	1,0 to	5,5	V [1]
Input base bias current	I_5, I_{13}	<	25	µA

Complete circuit

Total quiescent current with 3,3 kΩ between pins 7 and 8 (inclusive discrete input transistor, exclusive f.m. front end)	I_{tot}	typ. <	22 29	mA [2] mA [2]

1) Maximum input common mode voltage; V_{5-8}, V_{13-8}: < (V_P − 0,5) V.

2) In those cases where a lower supply current is required the resistor between pins 7 and 8 (3,3 kΩ) can be avoided, resulting in a total current of 17 mA. In this case however some devices may show a marginal increase of the distortion level.

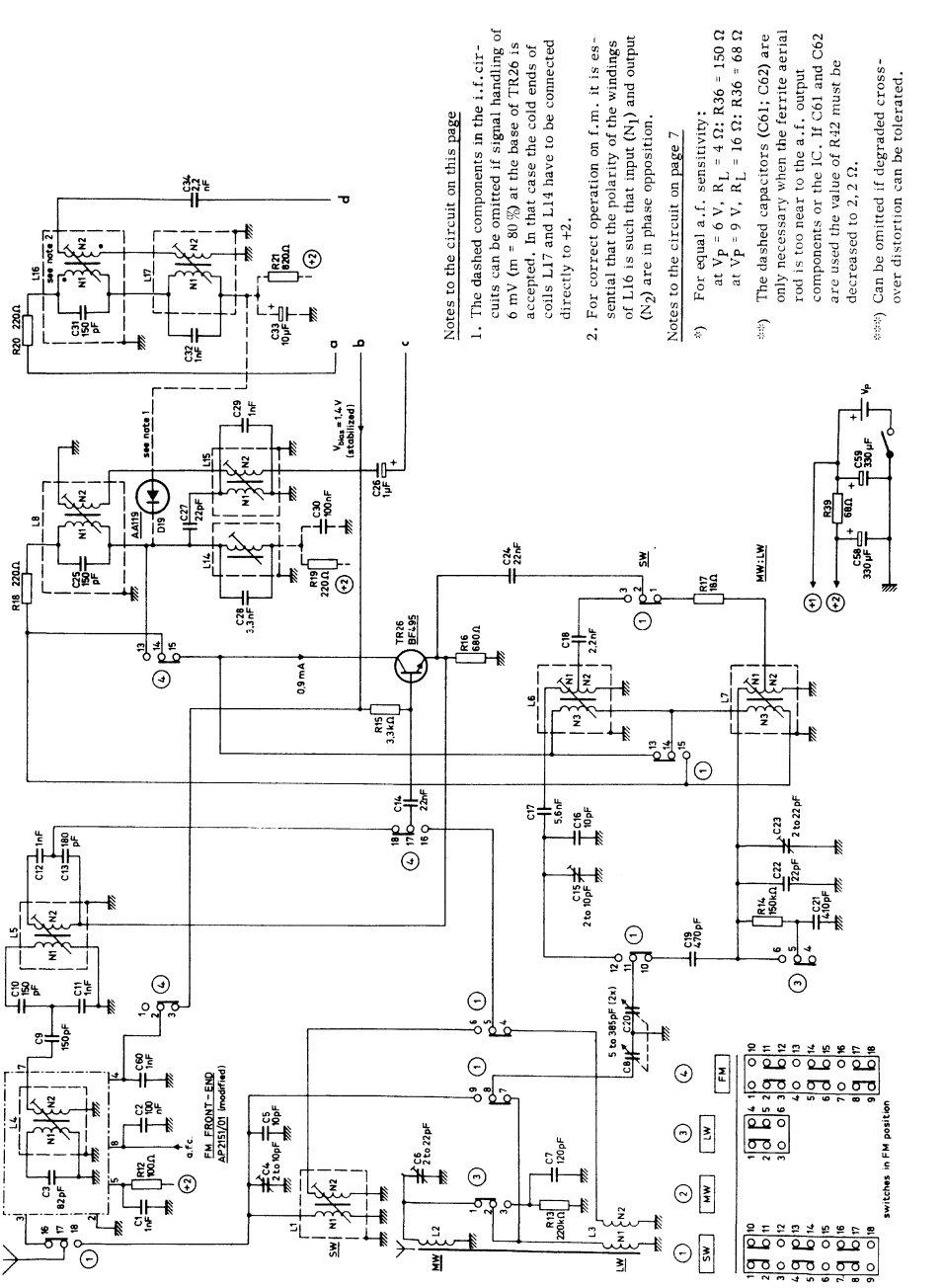
CHARACTERISTICS (continued)

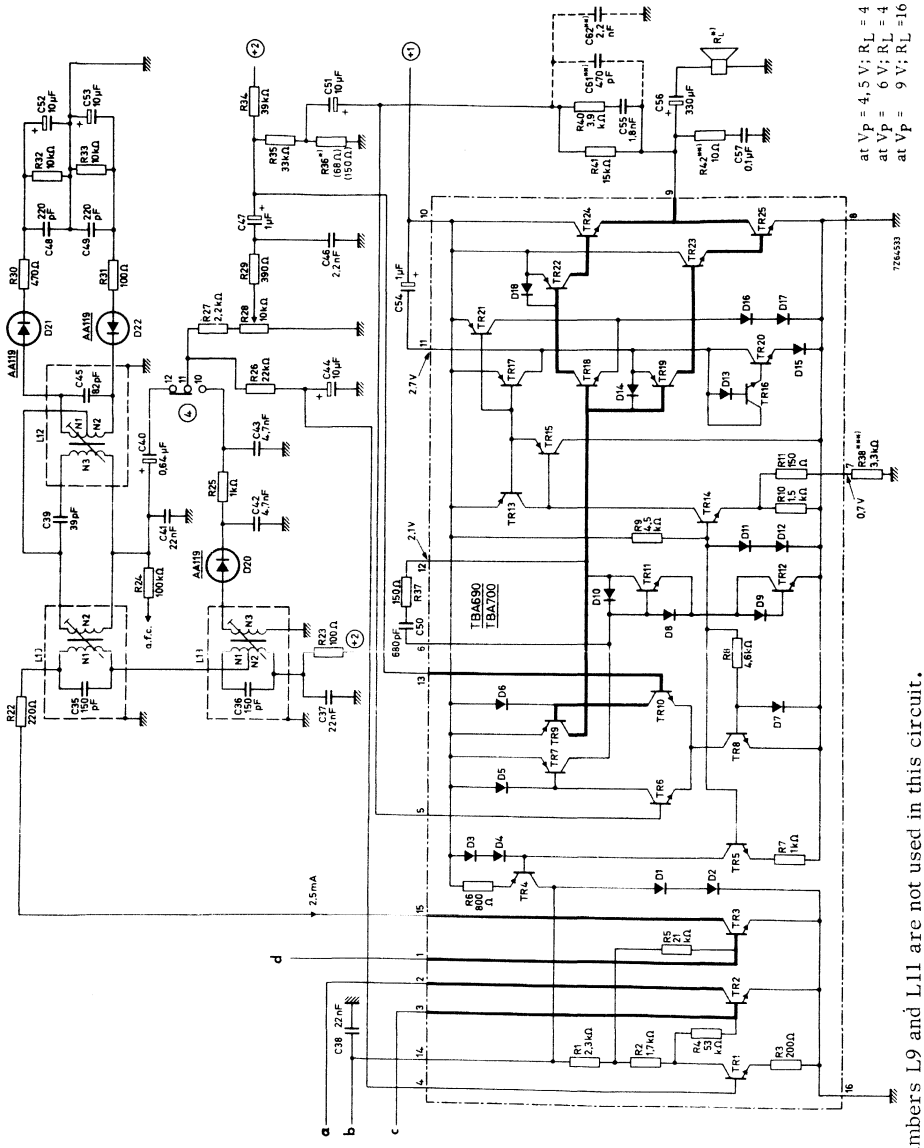
A.C. characteristics of i.f. part

y parameters at f = 450 kHz [1]		i.f. transistor: TR2		TR3	
Input conductance	g_{ie}	typ.	0,45	1,15	mA/V
Input capacitance	C_{ie}	typ.	23	36	pF
Output conductance	g_{oe}	typ.	6,0	13,5	μA/V
Output capacitance	C_{oe}	typ.	4,0	4,25	pF
Transfer admittance	$\|y_{fe}\|$	typ.	37	82	mA/V
Phase angle of transfer admittance	φ_{fe}	typ.	1°	2°	
Feedback admittance	$\|y_{re}\|$	typ.	2,5	1,8	μA/V
Phase angle of feedback admittance	φ_{re}	typ.	90°	90°	

y parameters at f = 10,7 MHz [1]		i.f. transistor: TR2		TR3	
Input conductance	g_{ie}	typ.	0,6	1,5	mA/V
Input capacitance	C_{ie}	typ.	22	35	pF
Output conductance	g_{oe}	typ.	24	30	μA/V
Output capacitance	C_{oe}	typ.	4,3	4,7	pF
Transfer admittance	$\|y_{fe}\|$	typ.	35	73	mA/V
Phase angle of transfer admittance	φ_{fe}	typ.	22°	35°	
Feedback admittance	$\|y_{re}\|$	typ.	64	43	μA/V
Phase angle of feedback admittance	φ_{re}	typ.	90°	90°	

1) At typical values for h_{fe} and I_c.


FM FRONT-END AP2151/01 (modified)
switches in FM position
SW
MW
LW
FM
MW+LW
TR26 BF495
AA119
0,9 mA
V_{bias} = 1,4 V (stabilized)
5 to 385 pF (2x)
see note 1
see note 2
a.f.c.
Notes to the circuit on this page
1. The dashed components in the i.f. circuits can be omitted if signal handling of 6 mV (m = 80 %) at the base of TR26 is accepted. In that case the cold ends of coils L17 and L14 have to be connected directly to +2.
2. For correct operation on f.m. it is essential that the polarity of the windings of L16 is such that input (N_1) and output (N_2) are in phase opposition.
Notes to the circuit on page 7
*) For equal a.f. sensitivity:
at V_P = 6 V, R_L = 4 Ω: R36 = 150 Ω
at V_P = 9 V, R_L = 16 Ω: R36 = 68 Ω
**) The dashed capacitors (C61; C62) are only necessary when the ferrite aerial rod is too near to the a.f. output components or the IC. If C61 and C62 are used the value of R42 must be decreased to 2,2 Ω.
***) Can be omitted if degraded cross-over distortion can be tolerated.



Reference numbers L9 and L11 are not used in this circuit.

APPLICATION INFORMATION (continued) at $T_{amb} = 25\ ^{o}C$; $V_p = 6$ V

See also circuit diagram on pages 6 and 7.

A.M. performance

R.F. input voltage for signal to noise ratio of 26 dB	V_i	typ.	15	μV	1)2)
R.F. input voltage for 10 mV (a.f.) across volume control	V_i	typ.	3	μV	1)2)
A.F. voltage across volume control at 100 μV (r.f.) input voltage	V_o	typ.	100	mV	1)2)
Signal to noise ratio at 1 mV (r.f.) input voltage	S/N	typ.	53,4	dB	1)2)
A.G.C. range (change in r.f. input voltage for 10 dB expansion in audio range)					
without a.g.c. diode		typ.	42	dB	1)2)3)
with a.g.c. diode		typ.	72	dB	1)2)
R.F. signal handling capability on base of TR26 80 % modulation ($d_{tot} \leq 10\ \%$)					
without a.g.c. diode	V_i	typ.	6	mV	3)
with a.g.c. diode	V_i	typ.	80	mV	
Harmonic distortion of h.f. part (over most of a.g.c. range)	d_{tot}	typ.	1	%	1)2)
I.F. selectivity	S_9	typ.	30	dB	
I.F. bandwidth	B_{3dB}	typ.	4,5	kHz	

1) a. Negligible influence of supply voltage variations in a range of 2,7 V to 12 V.
   b. A.F. signal: measured across volume control.
   c. R.F. signal: measured at base of external mixer-oscillator with the antenna-circuit connected (source resistance R_S of about 1 kΩ).
   d. $f_0 = 1$ MHz, $f_m = 1$ kHz
2) m = 0,3
3) Dashed parts of circuit diagram on pages 6 and 7 are omitted.

APPLICATION INFORMATION (continued) See also circuit on pages 6 and 7.

F.M. performance

Sensitivity for an f.m. signal 3 dB before limiting					
at 75 Ω aerial input of f.m. front end	V_i	typ.	8	μV	1)
at base of external (first i.f.) stage	V_i	typ.	100	μV	2)
at pin 3	V_i	typ.	1,8	mV	2)
Sensitivity for 26 dB S/N ratio at 75 Ω aerial input of f.m. front end	V_i	typ.	4	μV	1)
A.F. output voltage across volume control at an i.f. signal beyond limiting	V_o	typ.	100	mV	2)
S/N ratio over most of signal range	S/N	typ.	55	dB	2)
A.M. suppression over most of signal range		>	40	dB	2)3)
I.F. selectivity	S_{300}	typ.	40	dB	4)
I.F. bandwidth	B_{3dB}	typ.	180	kHz	4)
A.F. signal distortion, 3 dB before i.f. limiting	d_{tot}	<	2	%	5)

Audio performance

A.F. output power at d_{tot} = 10 %	P_o	typ.	0,6	W	6)
at onset of clipping	P_o	typ.	0,5	W	6)
Distortion before clipping	d_{tot}	typ.	1	%	6)
A.F. input signal (at pin 13)					
at P_o = 50 mW	V_i	typ.	6	mV	6)
at P_o = 500 mW	V_i	typ.	20	mV	6)
Noise output power (volume control at minimum)	P_N	typ.	20	nW	7)
Typical overall fidelity (flat within 3 dB)		200 Hz to	6	kHz	8)
Open loop voltage gain	G_v	typ.	60	dB	

1) Aerial e.m.f. (V_i) at f_o = 100 MHz; R_S = 50 Ω (source resistance; see page 12). $\Delta f = \pm 15$ kHz; f_m = 1 kHz.
2) f_o = 10,7 MHz; $\Delta f = \pm 15$ kHz; f_m = 1 kHz.
3) A.M. signal: m = 0,3; f_m = 400 Hz (carrier simultaneously modulated with a.m. and f.m.).
4) Including ratio detector.
5) f_o = 100 MHz; $\Delta f = \pm 40$ kHz; f_m = 1 kHz.
6) Measured at 1 kHz, a negative feedback of 20 dB and a loudspeaker of 4 Ω; V_P = 6 V.
7) Measured at a bandwidth of 200 Hz to 6 kHz, pin 13 being connected via a capacitor of 32 μF to pin 16; loudspeaker impedance 4 Ω.
8) Depending on values of capacitors C51 and C55, 50 Hz to 15 kHz is possible.

COIL DATA See also circuit on pages 6 and 7.

1. **A.M.–I.F. coils** (f_o = 452 kHz)

First i.f. bandpass filter

Primary : L14 = 38 μH
C_p = 3300 pF
Q_0 = 90

Secondary : L15 (N_1) = 125 μH
C_p = 1000 pF
Q_0 = 80
N_1/N_2 = 18
$kQ_{L14-L15}$ = 1

Single tuned coil

L17 (N_1) = 125 μH
C_p = 1000 pF
Q_0 = 80
N_1/N_2 = 30

Detector coil

L13 (N_1+N_2) = 0,84 mH
C_p = 150 pF
Q_0 = 130
N_1/N_2 = 3,1
$(N_1+N_2)/N_3$ = 4

2. **F.M.–I.F. coils** (f_o = 10,7 MHz)

First i.f. bandpass filter

Primary : L4 (N_1) = 2,6 μH
C_p = 82 pF
Q_0 = 90
N_1/N_2 = 10

Secondary : L5 (N_1) = 1,44 μH
C_p = 150 pF
Q_0 = 55
N_1/N_2 = 5,7
kQ_{L4-L5} = 1,2

First single tuned filter

L8 (N_1) = 1,44 μH
C_p = 150 pF
Q_0 = 45
N_1/N_2 = 5,7

Second single tuned filter

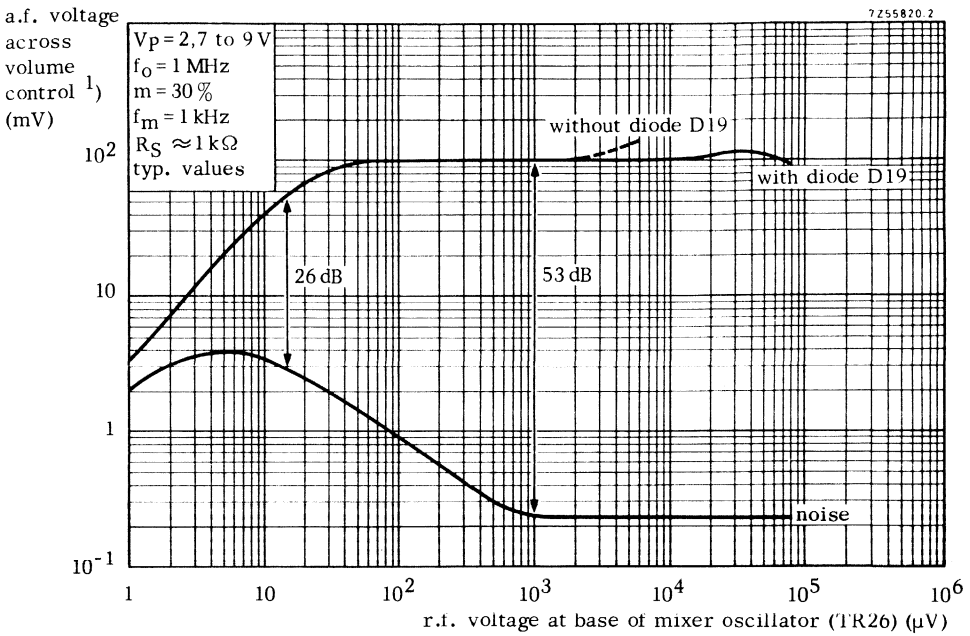
L16 (N_1) = 1,44 μH
C_p = 150 pF
Q_0 = 45
N_1/N_2 = 5,7

Ratio detector

Primary : L10 (N_1) = 1,44 μH
C_p = 150 pF
Q_0 = 95
N_1/N_2 = 2

Secondary : L12 (N_1+N_2) = 2,6 μH
C_p = 82 pF
Q_0 = 110
N_1/N_2 = 1
$(N_1+N_2)/N_3$ = 5,4
$kQ_{L10-L12}$ = 0,7

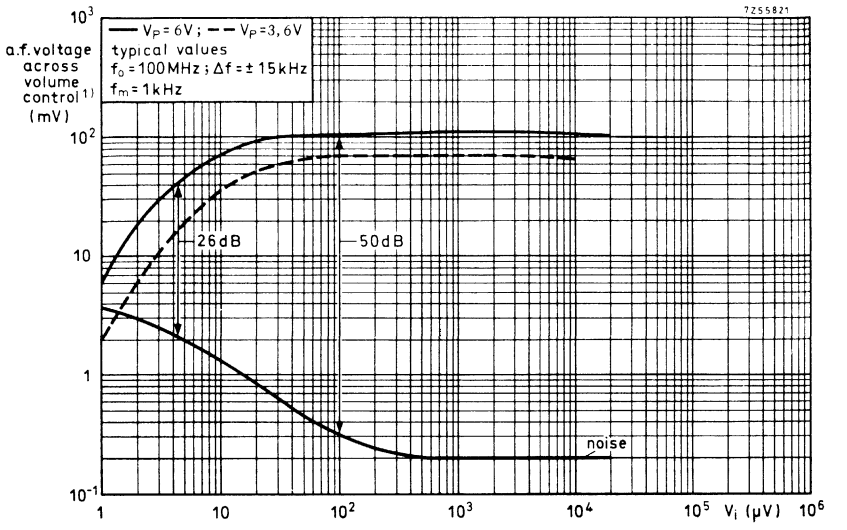
APPLICATION INFORMATION (continued)



Typical a.g.c. curves at a.m. reception

A.F. voltage across volume control versus r.f. voltage at base of mixer-oscillator.

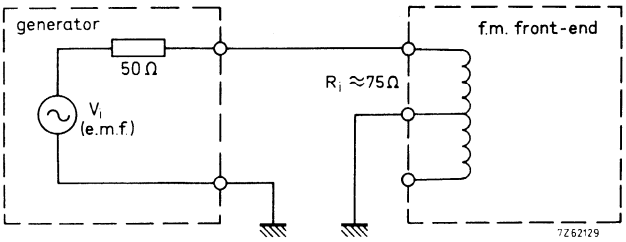
APPLICATION INFORMATION (continued)



Typical S/N curves at f.m. reception

A.F. voltage across volume control versus aerial e.m.f. represented by the generator voltage V_i (e.m.f.) connected to the 75 Ω input of the f.m. front-end.

Test circuit



1) Slider at lower end.

INTEGRATED A.M./F.M. RADIO RECEIVER CIRCUIT

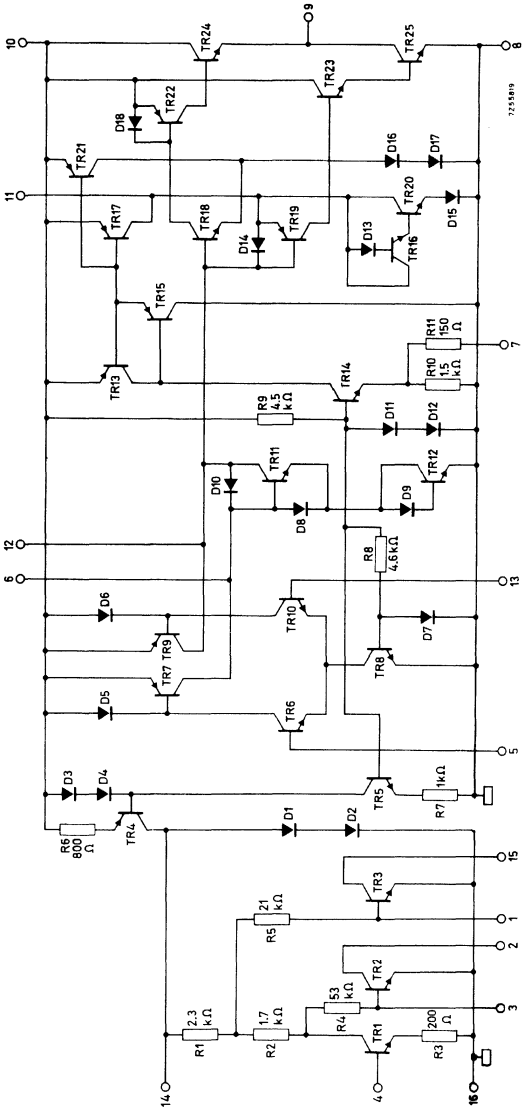
The TBA700 is a monolithic integrated circuit for use in a.m. (including the short-wave band), a.m./f.m. receivers.
It incorporates the class-B audio output stage (1 W), stabilization circuit for quiescent current, driver, pre-amplifier, 2-stage i.f. amplifier, a.g.c. and stabilized bias circuit.
The discrete input stage (for a.m.: mixer-oscillator; for f.m.: 1st i.f.) enables a high flexibility in circuit lay-out with conventional or lumped selectivity.
The internal stabilization ensures negligible loss of sensitivity and cross-over distortion over a wide supply voltage range from 2,7 V to 12 V.

QUICK REFERENCE DATA				
Applicable supply voltage range of receiver	V_{10-8}		2,7 to 12	V [1]
Ambient temperature	T_{amb}		25	°C
Supply voltage	V_P	nom.	9	V
Total quiescent current (inclusive discrete input transistor, exclusive f.m. front end)	I_{tot}	typ.	24,5	mA
A.F. output power at d_{tot} = 10 %, R_L = 8 Ω	P_o	typ.	1000	mW
A.M. performance				
R.F. input voltage (S/N = 26 dB) (at base of external mixer-oscillator)	V_i	typ.	15	μV
A.G.C. range (change of r.f. input voltage for 10 dB expansion in audio range)		typ.	72	dB
F.M. performance				
R.F. input voltage (at base of external i.f. stage) 3 dB before limiting	V_i	typ.	150	μV

PACKAGE OUTLINE 16 lead plastic dual in-line with internal copper slug (type A) (See General Section)

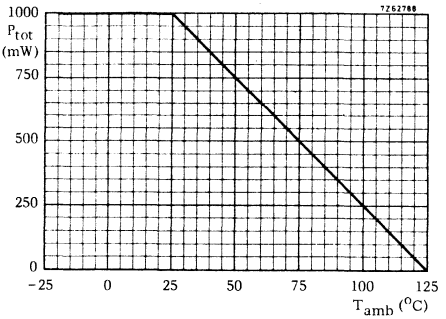
1) The data given in this sheet are based on a receiver with V_P = 9 V; P_o = 1000 mW.

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages					
Pin No. 10 voltage	V_{10-8}	max.	12	V	
Pins No. 15, 9, 2 voltages	V_{15-8}, V_{9-8}, V_{2-8}	max.	11,4	V	
Pin No. 16 voltage	V_{16-8}	max.	0	V	1)
Pin No. 7 voltage	$\pm V_{7-8}$	max.	5	V	
Pins No. 4, 3, 1 voltages	$-V_{4-16}$, $-V_{3-16}$, $-V_{1-16}$	max.	5	V	
Pin No. 5 voltage	$\pm V_{5-13}$	max.	5	V	
Pin No. 10 voltage	V_{10-9}	max.	11,4	V	
Currents					
Pins No. 14, 12, 11, 6 currents	$I_{14}, I_{12}, I_{11}, I_6$	max.	5	mA	
Pins No. 13, 5, 4, 3, 1 currents	$I_{13}, I_5, I_4, I_3, I_1$	max.	0,5	mA	
Pins No. 15, 2 currents	I_{15}, I_2	max.	10	mA	
Pin No. 8 current	$-I_{8RM}$	max.	0,8	A	2)
Pin No. 9 current	$\pm I_{9RM}$	max.	0,8	A	2)
Pin No. 10 current	I_{10RM}	max.	0,8	A	2)
Dissipation					
Total power dissipation					
at T_{amb} = 45 °C	P_{tot}	max.	800	mW	
at T_{amb} = 25 °C	P_{tot}	max.	1000	mW	
Temperatures					
Storage temperature	T_{stg}		−55 to +125	°C	
Operating ambient temperature	T_{amb}		−20 to +125	°C	



1) Substrate connected to pin 16.
2) Repetitive peak value; internally limited.

CHARACTERISTICS

D.C. characteristics at $T_{amb} = 25\ ^{o}C$; $V_P = 9$ V

I. F. amplifier

Collector current of i.f. transistor TR2 (a.g.c. transistor "off")	I_C	typ.	1	mA
			0,55 to 1,6	mA
Collector current of i.f. transistor TR3 (a.g.c. transistor "off")	I_C	typ.	2,5	mA
			1,4 to 4,2	mA
Saturation voltage of i.f. transistor TR2 at $I_C \leq 2$ mA	V_{CEsat}	<	150	mV
Saturation voltage of i.f. transistor TR3 at $I_C \leq 5$ mA	V_{CEsat}	<	200	mV
Bias voltage for mixer and tuner	V_{14-16}	typ.	1,4	V
			1,25 to 1,55	V
Temperature dependency of bias voltage V_{14-16}	T_c	typ.	-3,6	mV/°C
Bias current (available)	$-I_{14}$	<	100	μA

A. F. amplifier

Input common mode voltage range	V_{5-8}, V_{13-8}		1,0 to 8,5	V [1]
Input base bias current	I_5, I_{13}	<	25	μA

Complete circuit

Total quiescent current with 3,3 kΩ between pins 7 and 8 (inclusive discrete input transistor, exclusive f.m. front end)	I_{tot}	typ.	24,5	mA [2]
		<	30,5	mA [2]

1) Maximum input common mode voltage; V_{5-8}, V_{13-8}: $< (V_P - 0,5)$ V.

2) In those cases where a lower supply current is required the resistor between pins 7 and 8 (3,3 kΩ) can be avoided, resulting in a total current of 17 mA. In this case however some devices may show a marginal increase of the distortion level.

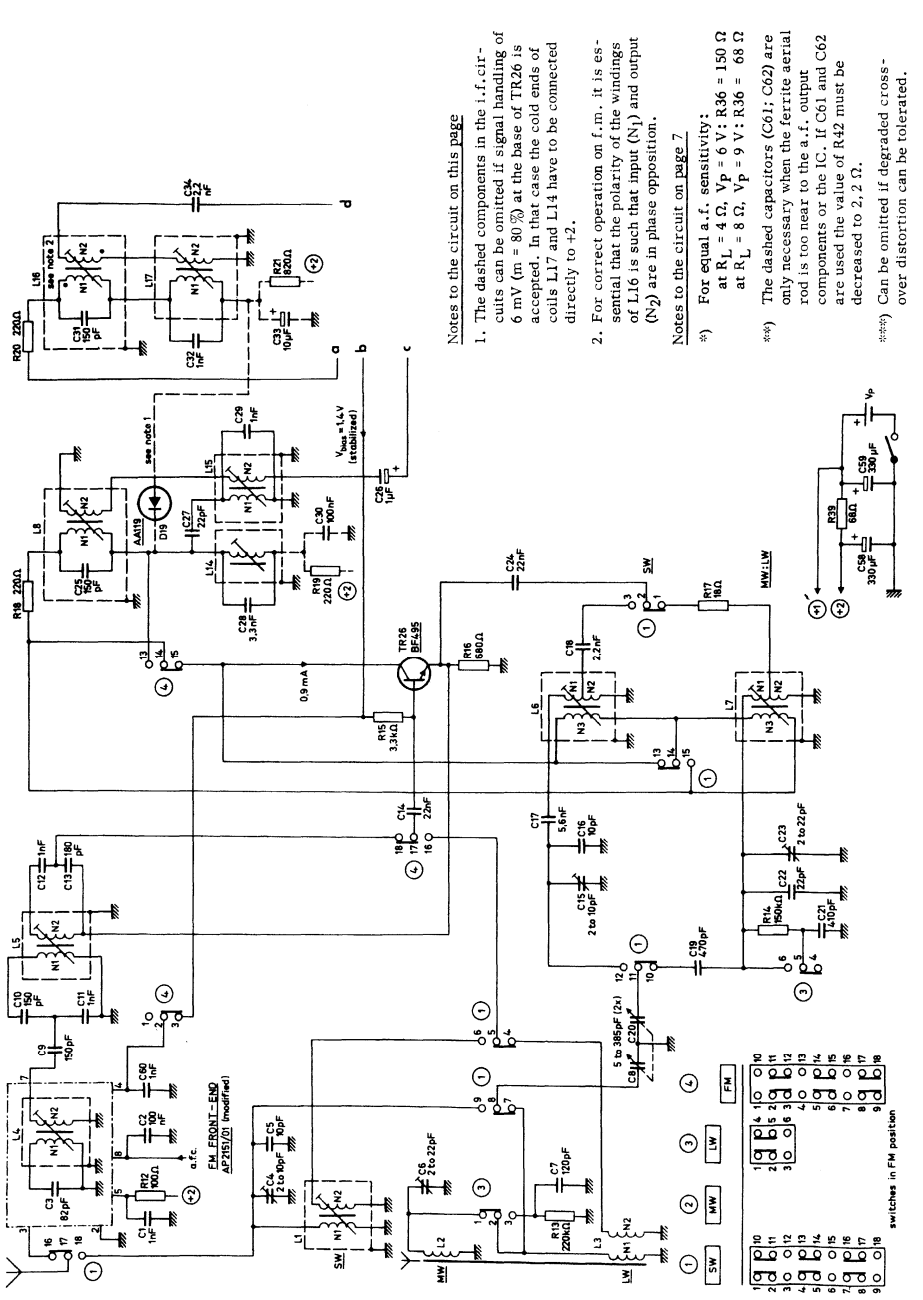
CHARACTERISTICS (continued)

A.C. characteristics of i.f. part

y parameters at f = 450 kHz [1]	i.f. transistors:		TR2	TR3	
Input conductance	g_{ie}	typ.	0,45	1,15	mA/V
Input capacitance	C_{ie}	typ.	23	36	pF
Output conductance	g_{oe}	typ.	6,0	13,5	μA/V
Output capacitance	C_{oe}	typ.	4,0	4,25	pF
Transfer admittance	$\|y_{fe}\|$	typ.	37	82	mA/V
Phase angle of transfer admittance	φ_{fe}	typ.	1^o	2^o	
Feedback admittance	$\|y_{re}\|$	typ.	2,5	1,8	μA/V
Phase angle of feedback admittance	φ_{re}	typ.	90^o	90^o	

y parameters at f = 10,7 MHz [1]	i.f. transistors:		TR2	TR3	
Input conductance	g_{ie}	typ.	0,6	1,5	mA/V
Input capacitance	C_{ie}	typ.	22	35	pF
Output conductance	g_{oe}	typ.	24	30	μA/V
Output capacitance	C_{oe}	typ.	4,3	4,7	pF
Transfer admittance	$\|y_{fe}\|$	typ.	35	73	mA/V
Phase angle of transfer admittance	φ_{fe}	typ.	22^o	35^o	
Feedback admittance	$\|y_{re}\|$	typ.	64	43	μA/V
Phase angle of feedback admittance	φ_{re}	typ.	90^o	90^o	

1) At typical values for h_{fe} and I_c.



Notes to the circuit on this page

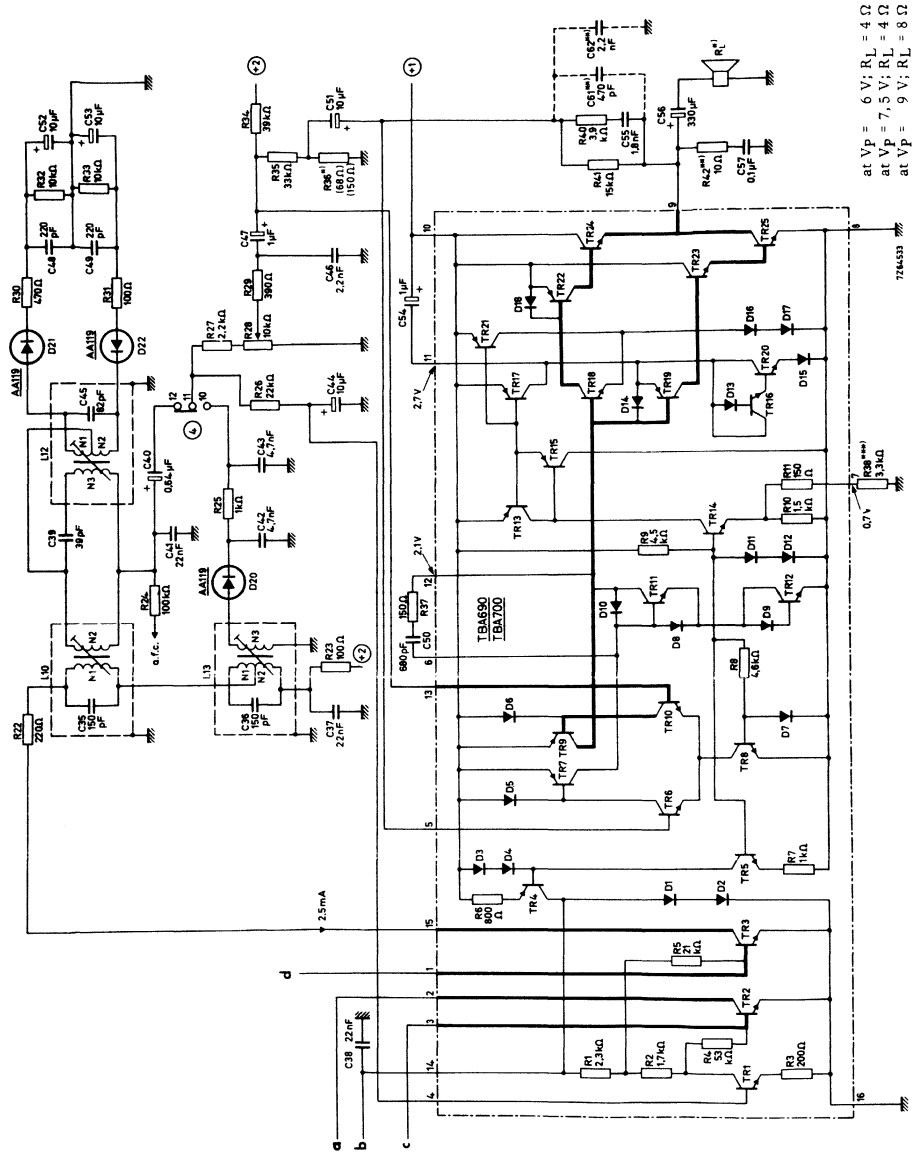
1. The dashed components in the i.f. circuits can be omitted if signal handling of 6 mV (m = 80 %) at the base of TR26 is accepted. In that case the cold ends of coils L17 and L14 have to be connected directly to +2.
2. For correct operation on f.m. it is essential that the polarity of the windings of L16 is such that input (N_1) and output (N_2) are in phase opposition.

Notes to the circuit on page 7

*) For equal a.f. sensitivity:
at R_L = 4 Ω, Vp = 6 V: R36 = 150 Ω
at R_L = 8 Ω, Vp = 9 V: R36 = 68 Ω

**) The dashed capacitors (C61; C62) are only necessary when the ferrite aerial rod is too near to the a.f. output components or the IC. If C61 and C62 are used the value of R42 must be decreased to 2,2 Ω.

***) Can be omitted if degraded cross-over distortion can be tolerated.



Reference numbers L9 and L11 are not used in this circuit.

APPLICATION INFORMATION (continued) at T_{amb} = 25 °C; V_P = 9 V

See also circuit diagram on pages 6 and 7.

A.M. performance

R.F. input voltage for signal to noise ratio of 26 dB	V_i	typ.	15	μV	1)2)
R.F. input voltage for 10 mV (a.f.) across volume control	V_i	typ.	3	μV	1)2)
A.F. voltage across volume control at 100 μV (r.f.) input voltage	V_o	typ.	100	mV	1)2)
Signal to noise ratio at 1 mV (r.f.) input voltage	S/N	typ.	53,4	dB	1)2)
A.G.C. range (change in r.f. input voltage for 10 dB expansion in audio range)					
without a.g.c. diode		typ.	42	dB	1)2)3)
with a.g.c. diode		typ.	72	dB	1)2)
R.F. signal handling capability on base of TR26 80 % modulation ($d_{tot} \leq 10$ %)					
without a.g.c. diode	V_i	typ.	6	mV	3)
with a.g.c. diode	V_i	typ.	80	mV	
Harmonic distortion of h.f. part (over most of a.g.c. range)	d_{tot}	typ.	1	%	1)2)
I.F. selectivity	S_9	typ.	30	dB	
I.F. bandwidth	B_{3dB}	typ.	4,5	kHz	

1) a. Negligible influence of supply voltage variations in a range of 2,7 V to 12 V
   b. A.F. signal: measured across volume control.
   c. R.F. signal: measured at base of external mixer-oscillator with the antenna-circuit connected (source resistance R_S of about 1 kΩ).
   d. f_o = 1 MHz, f_m = 1 kHz
2) m = 0.3
3) Dashed parts of circuit diagram on pages 6 and 7 are omitted.

APPLICATION INFORMATION (continued) See also circuit on pages 6 and 7.

F.M. performance

Sensitivity for an f.m. signal 3 dB before limiting					
at 75 Ω aerial input of f.m. front end	V_i	typ.	12	μV	1)
at base of external (first i.f.) stage	V_i	typ.	150	μV	2)
at pin 3	V_i	typ.	2,2	mV	2)
Sensitivity for 26 dB S/N ratio					
at 75 Ω aerial input of f.m. front end	V_i	typ.	4	μV	1)
A.F. output voltage across volume control at an i.f. signal beyond limiting	V_o	typ.	140	mV	2)
S/N ratio over most of signal range	S/N	typ.	55	dB	2)
A.M. suppression over most of signal range		>	40	dB	2)3)
I.F. selectivity	S_{300}	typ.	40	dB	4)
I.F. bandwidth	B_{3dB}	typ.	180	kHz	4)
A.F. signal distortion, 3 dB before i.f. limiting	d_{tot}	<	2	%	5)

Audio performance

A.F. output power at d_{tot} = 10 %	P_o	typ.	1	W	6)
at onset of clipping	P_o	typ.	0,7	W	6)
Distortion before clipping	d_{tot}	typ.	1	%	6)
A.F. input signal (at pin 13)					
at P_o = 50 mW	V_i	typ.	6	mV	6)
at P_o = 700 mW	V_i	typ.	17	mV	6)
Noise output power (volume control at minimum)	P_N	typ.	20	nW	7)
Typical overall fidelity (flat within 3 dB)		200 Hz to	6	kHz	8)
Open loop voltage gain	G_v	typ.	60	dB	

1) Aerial e.m.f. (V_i) at f_o = 100 MHz; R_S = 50 Ω (source resistance; see page 12) $\Delta f = \pm 15$ kHz; f_m = 1 kHz.
2) f_o = 10,7 MHz; $\Delta f = \pm 15$ kHz; f_m = 1 kHz.
3) A.M. signal: m = 0,3; f_m = 400 Hz (carrier simultaneously modulated with a.m. and f.m.).
4) Including ratio detector.
5) f_o = 100 MHz; $\Delta f = \pm 40$ kHz; f_m = 1 kHz.
6) Measured at 1 kHz, a negative feedback of 15 dB and a loudspeaker of 8 Ω; V_P = 9 V.
7) Measured at a bandwidth of 200 Hz to 6 kHz, pin 13 being connected via a capacitor of 32 μF to pin 16; loudspeaker impedance 8 Ω.
8) Depending on values of capacitors C51 and C55, 50 Hz to 15 kHz is possible.

COIL DATA See also circuit on pages 6 and 7.

1. **A.M.–I.F. coils** (f_o = 452 kHz)

First i.f. bandpass filter

Primary : L14 = 38 μH
C_p = 3300 pF
Q_0 = 90

Secondary : L15 (N_1) = 125 μH
C_p = 1000 pF
Q_0 = 80
N_1/N_2 = 18
$kQ_{L14\text{-}L15}$ = 1

Single tuned coil

L17 (N_1) = 125 μH
C_p = 1000 pF
Q_0 = 80
N_1/N_2 = 30

Detector coil

L13 (N_1+N_2) = 0, 84 mH
C_p = 150 pF
Q_0 = 130
N_1/N_2 = 3, 1
$(N_1+N_2)/N_3$ = 4

2. **F.M.–I.F. coils** (f_o = 10, 7 MHz)

First i.f. bandpass filter

Primary : L4 (N_1) = 2, 6 μH
C_p = 82 pF
Q_0 = 90
N_1/N_2 = 10

Secondary : L5 (N_1) = 1, 44 μH
C_p = 150 pF
Q_0 = 55
N_1/N_2 = 5, 7
$kQ_{L4\text{-}L5}$ = 1, 2

First single tuned filter

L8 (N_1) = 1, 44 μH
C_p = 150 pF
Q_0 = 45
N_1/N_2 = 5, 7

Second single tuned filter

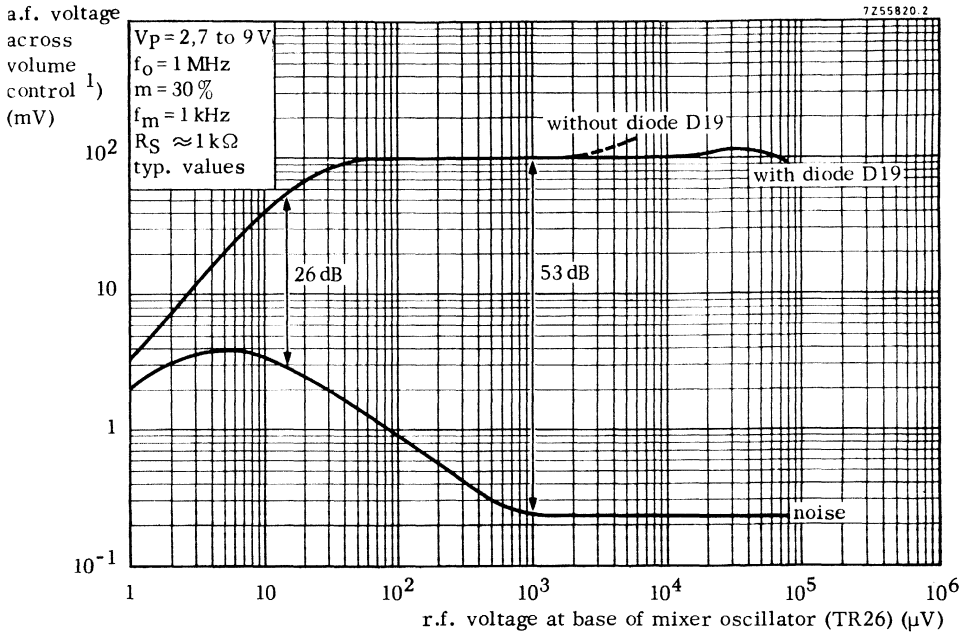
L16 (N_1) = 1, 44 μH
C_p = 150 pF
Q_0 = 45
N_1/N_2 = 5, 7

Ratio detector

Primary : L10 (N_1) = 1, 44 μH
C_p = 150 pF
Q_0 = 95
N_1/N_2 = 2

Secondary : L12 (N_1+N_2) = 2, 6 μH
C_p = 82 pF
Q_0 = 110
N_1/N_2 = 1
$(N_1+N_2)/N_3$ = 5, 4
$kQ_{L10\text{-}L12}$ = 0, 7

APPLICATION INFORMATION (continued)

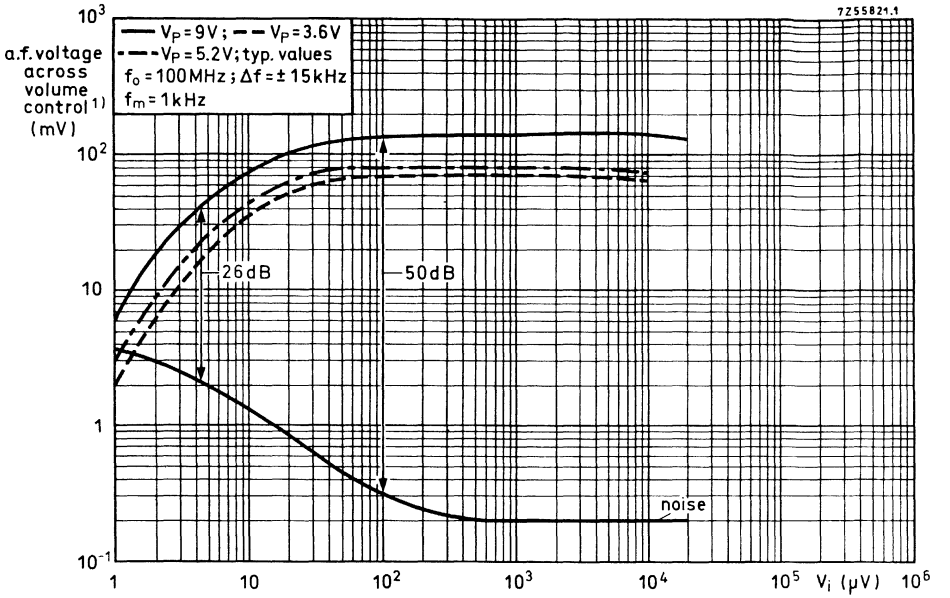


Typical a.g.c. curves at a.m. reception

A.F. voltages across volume control versus r.f. voltage at base of mixer-oscillator.

1) Slider at lower end.

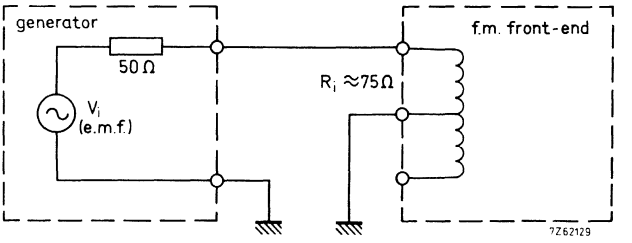
APPLICATION INFORMATION (continued)



Typical S/N curves at f.m. reception

A.F. voltage across volume control versus aerial e.m.f. represented by the generator voltage V_i (e.m.f.) connected to the 75 Ω input of the f.m. front-end.

Test circuit



1) Slider at lower end.

LINE OSCILLATOR CIRCUIT

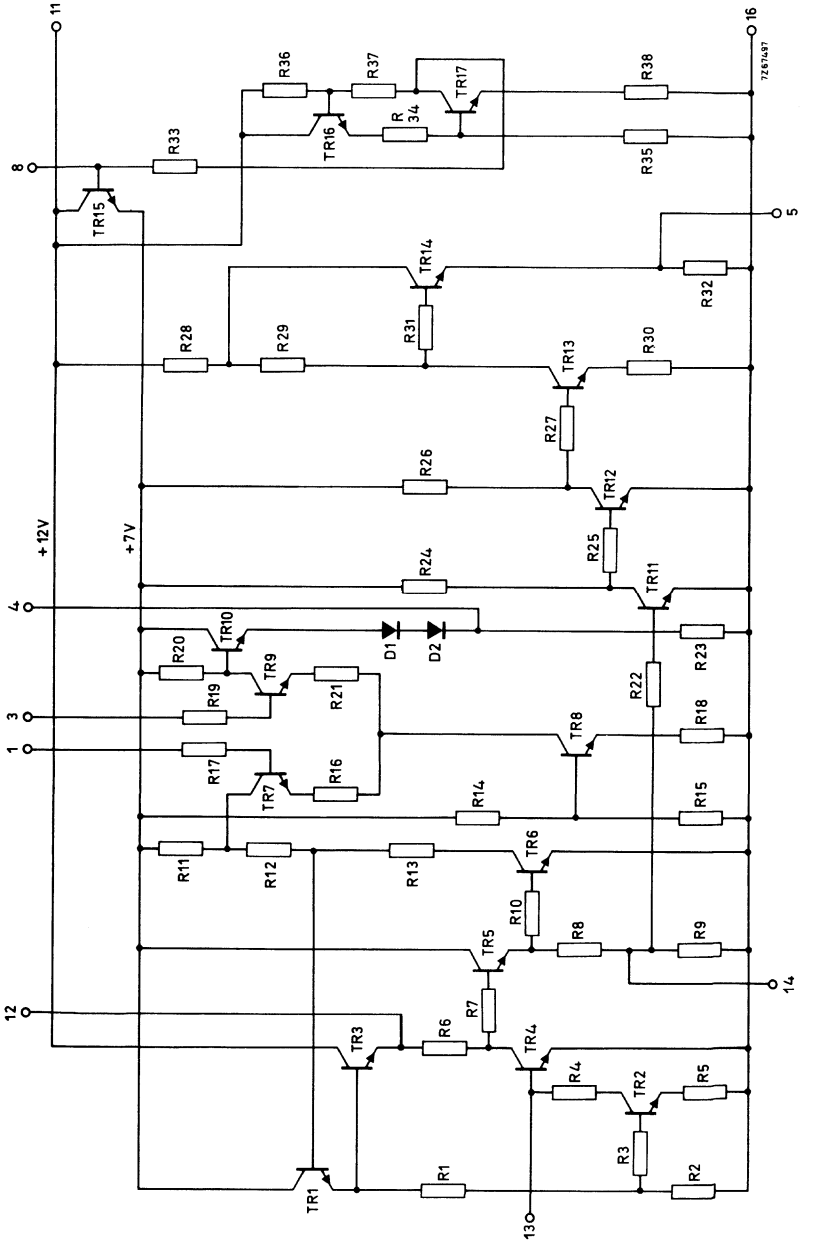
This circuit has been designed for use as line-oscillator and reactance stage in colour and monochrome t.v. receivers.
The circuit consists of a Miller-integrator-oscillator followed by a pulse shaping circuit, which delivers a positive pulse of 8 V and adjustable width.
The TBA720 can co-operate with the TBA890, TBA900, TAA700 and TBA550.

QUICK REFERENCE DATA				
Supply voltage	V_{11-16}	typ.	12	V
Required input signals				
D.C. control voltage at pin No. 1	V_{1-16}		2,4 to 5,3	V
at pin No. 3	V_{3-16}		2,4 to 5,3	V
Delivered output signals				
Output voltage at pin No. 5 no load; peak-to-peak value	$V_{5-16(p-p)}$	typ.	8	V
Output current at pin No. 5	I_5		10	mA

PACKAGE OUTLINE

TBA720 : 16 lead plastic dual in-line (type A) (See General Section)
TBA720Q : 16 lead plastic quadruple in-line (See General Section)

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Voltage				
Supply voltage	V_{11-16}	max.	16	V
Current				
Output current	I_5	max.	10	mA
Power dissipation				
Total power dissipation when mounted on a printed-wiring board	P_{tot}	max.	280	mW [1]
Temperatures				
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +60	°C

CHARACTERISTICS Measured in the test set-up on page 4

Supply voltage	V_{11-16}	typ.	12	V
			10 to 13	V
CHARACTERISTICS at T_{amb} = 25 °C; V_{11-16} = 12 V				
Supply current [2]	I_{11}	typ.	10	mA
			6,6 to 13,6	mA
Required input signals				
D.C. control voltage for nominal frequency at pin No. 1 and pin No. 3	$V_{1-16} = V_{3-16}$	typ.	3	V
			2,4 to 5,3	V
Sensitivity of reactance stage	V_{1-3}	typ.	2	kHz/V
Duty cycle regulation at pin No. 14	I_{14}	typ.	0	μA
			+200 to −650	μA
Delivered output signals				
Output voltage at pin No. 5 no load; peak-to-peak value	$V_{5-16(p-p)}$	typ.	10	V
Duty cycle	δ	typ.	20	%
Duty cycle; regulation range	δ		10 to 60	%
Rise time at pin No. 5 of leading edge of output pulse	t_r	typ.	200	ns

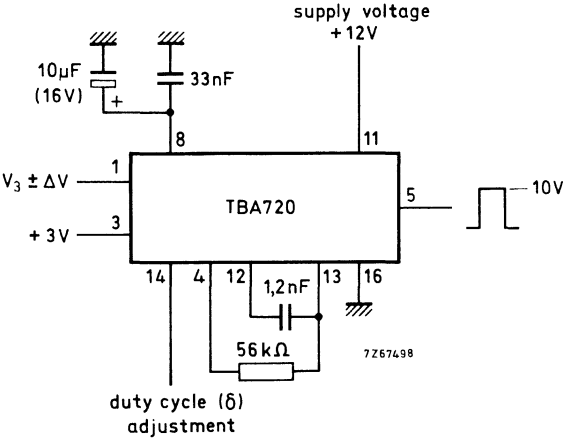
[1] Total dissipation for t < 60 s is 320 mW.

[2] No load connected to the output. When the output is loaded, the extra current is: $\delta \times I$, in which δ = duty cycle of output pulse and I = current flowing during output pulse.

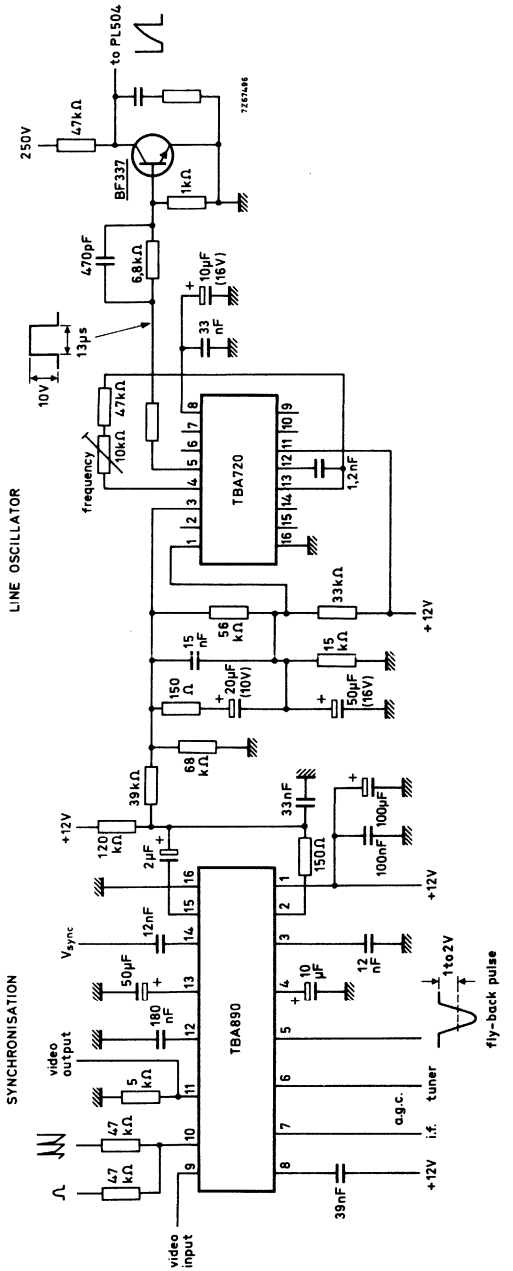
CHARACTERISTICS (continued)

Relative frequency deviation for ΔV_{11} = 1 V		max.	0,2	%
Relative frequency deviation for change of ambient temperature 25 to 55 °C		typ.	0,3	%
Allowable hum-ripple on supply line (peak-to-peak value)	$\Delta V_{11\text{-}16(p\text{-}p)}$	typ.	100	mV

Test set-up



APPLICATION INFORMATION



APPLICATION INFORMATION (continued)

Notes

1. The TBA720 is intended to drive a line deflection circuit equipped with tubes; for transistor-equipped deflection circuits the TBA720A should be used.
2. The duty cycle δ can be adjusted by connecting a resistor between pin 14 and earth.
3. The oscillation frequency can be set between 10 kHz and 25 kHz by connecting a resistor between pins 4 and 13, and a capacitor between pins 12 and 13.
4. At a nominal oscillation frequency of 15,625 kHz, the frequenty deviation is limited to ± 1,3 kHz to safeguard the line timebase output circuits.
5. Pins 2, 6, 7, 9, 10 and 15 should not be connected.

LINE OSCILLATOR CIRCUIT

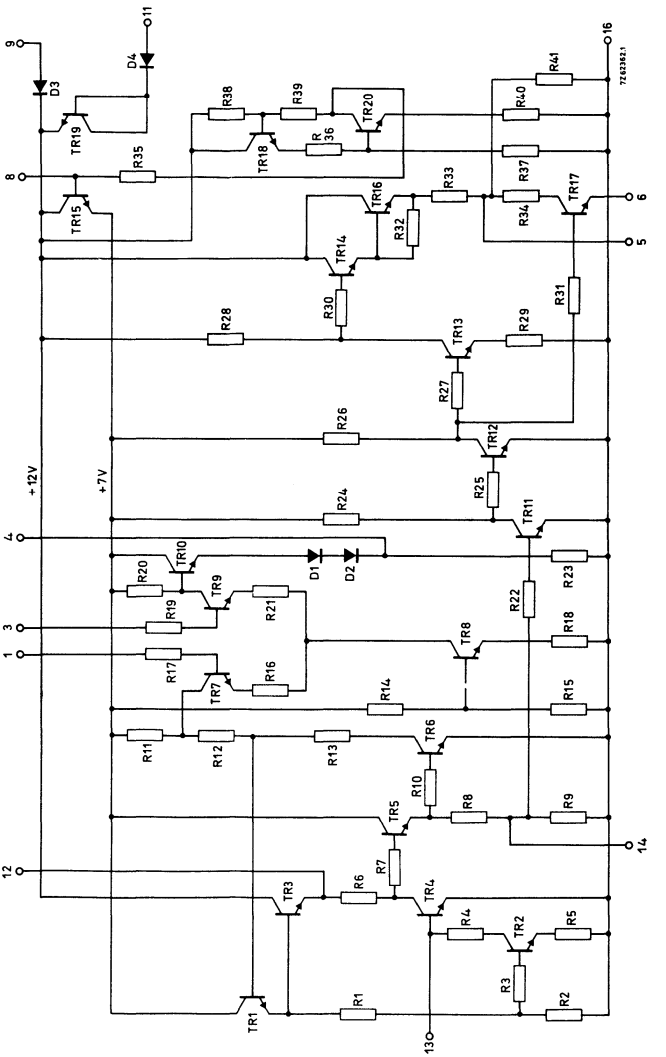
This circuit has been designed for use as line-oscillator and reactance stage in colour and monochrome t.v. receivers.
The circuit consists of a Miller-integrator-oscillator followed by a pulse shaping circuit, which delivers a positive pulse of 8 V and adjustable width. The available output current is in excess of 60 mA. Finally a supply voltage take-over switch for starting purposes is built in. The TBA720A can co-operate with the TBA890, TBA900, TAA700 and TBA550.

QUICK REFERENCE DATA			
Supply voltage	V_{11-16}	typ.	12 V
Starting voltage	V_{9-16}		8 to 12 V
Required input signals			
D.C. control voltage at pin No. 1	V_{1-16}		2,4 to 5,3 V
at pin No. 3	V_{3-16}		2,4 to 5,3 V
Delivered output signals			
Output voltage at pin No. 5 no load; peak-to-peak value	$V_{5-16(p-p)}$	typ.	8 V
Output current at pin No. 5	I_5	<	60 mA

PACKAGE OUTLINE

TBA720A : 16 lead plastic dual in-line (type A) (See General Section)
TBA720AQ: 16 lead plastic quadruple in-line (See General Section)

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Voltages			
Supply voltage	V_{11-16}	max.	16 V
Starting voltage	V_{9-16}	max.	15 V
Currents			
Output current	I_5	max.	60 mA
Power dissipation			
Total power dissipation when mounted on a printed-wiring board	P_{tot}	max.	280 mW
Temperatures			
Storage temperature	T_{stg}		−55 to +125 °C
Operating ambient temperature	T_{amb}		0 to +60 °C

CHARACTERISTICS Measured in the test set-up on page 4

Supply voltage	V_{11-16}	typ.	12 V 10 to 13 V
Starting voltage	V_{9-16}	>	8 V [1]

CHARACTERISTICS at T_{amb} = 25 °C; V_{11-16} = 12 V

Supply current [2]	I_{11}	typ.	10,5 mA 7,5 to 13,5 mA
Required input signals			
D.C. control voltage for nominal frequency at pin No. 1 and pin No. 3	$V_{1-16} = V_{3-16}$		2,4 to 5,3 V
Sensitivity of reactance stage	V_{1-3}	typ.	2 kHz/V
Duty cycle regulation at pin No. 14	I_{14}	typ.	0 μA +400 to −400 μA
Delivered output signals			
Output voltage at pin No. 5 no load; peak-to-peak value	$V_{5-16(p-p)}$	typ.	8 V
Output current	I_5	<	60 mA
Duty cycle; without regulation	δ	typ.	40 % 35 to 45 %
with regulation	δ		20 to 60 %
Rise time at pin No. 5 leading edge of output pulse	t_r	typ.	200 ns

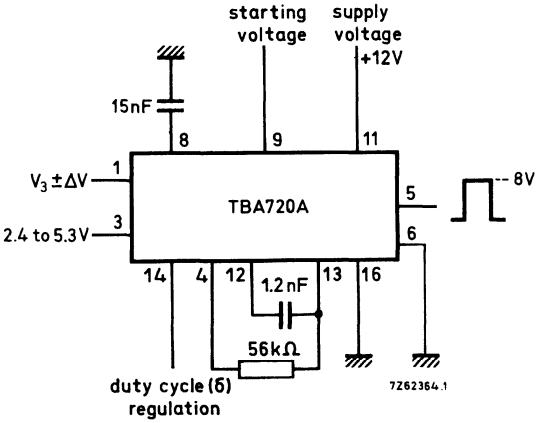
[1] Maximum starting voltage should not exceed the value of the supply voltage minus 1 volt.

[2] No load connected to the output. When the output is loaded, the extra current is: δ x I, in which δ = duty cycle of output pulse and I = current flowing during output pulse.

CHARACTERISTICS (continued)

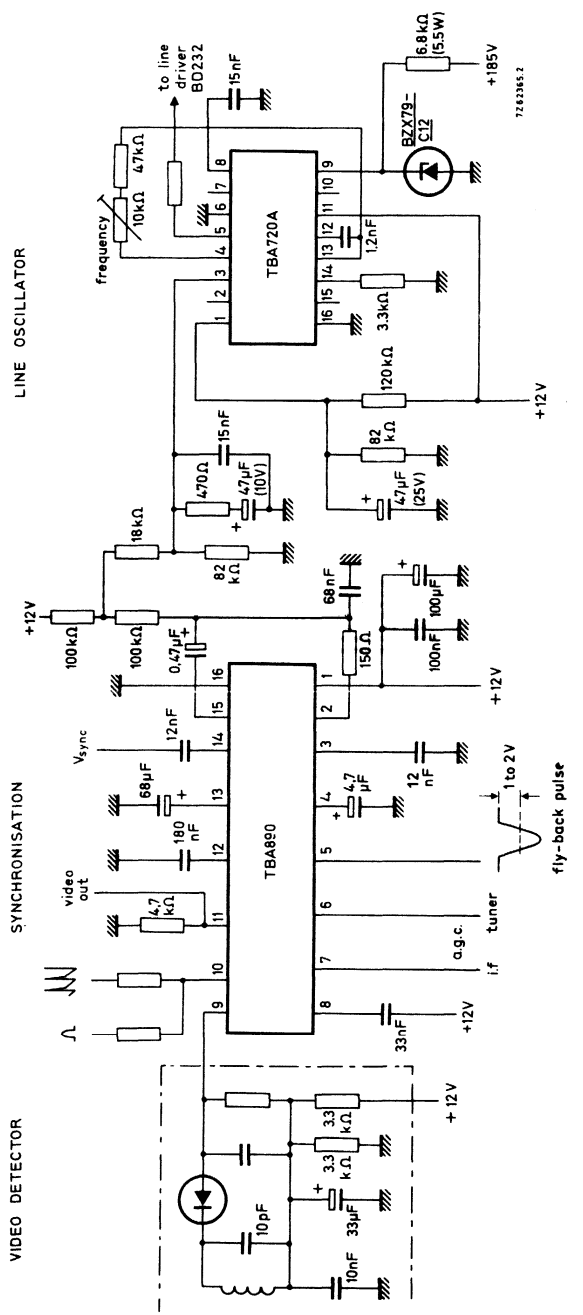
Relative frequency deviation for $\Delta V_{11} = 1$ V			2 ‰
Relative frequency deviation for change of ambient temperature 25 to 55 °C			3 ‰
Allowable hum-ripple on supply line (peak-to-peak value)	$\Delta V_{11-16(p-p)}$	typ.	100 mV

Test set-up



APPLICATION INFORMATION

The TBA720A with the TBA890 or TBA900 in a receiver with transistorized line deflection.



APPLICATION INFORMATION (continued)

Notes

1. The TBA720A is intended to drive a line deflection circuit equipped with transistors.
2. The duty cycle δ can be adjusted by connecting a resistor between pin 14 and ground or the supply.
3. The oscillation frequency can be set between 10 kHz and 25 kHz by connecting a resistor between pins 4 and 13, and a capacitor between pins 12 and 13.
4. At a nominal oscillation frequency of 15,625 kHz, the frequency deviation is limited to $\pm$1,3 kHz to safeguard the line timebase output circuits.
5. Besides the oscillator, the TBA720A incorporates a reactance stage and a supply voltage take-over switch for starting purposes (pin 9). The latter can be used to advantage if the 12 V supply is derived from the line flyback pulse.
6. Pins 2, 7, 10 and 15 should not be connected.

LIMITER-AMPLIFIER

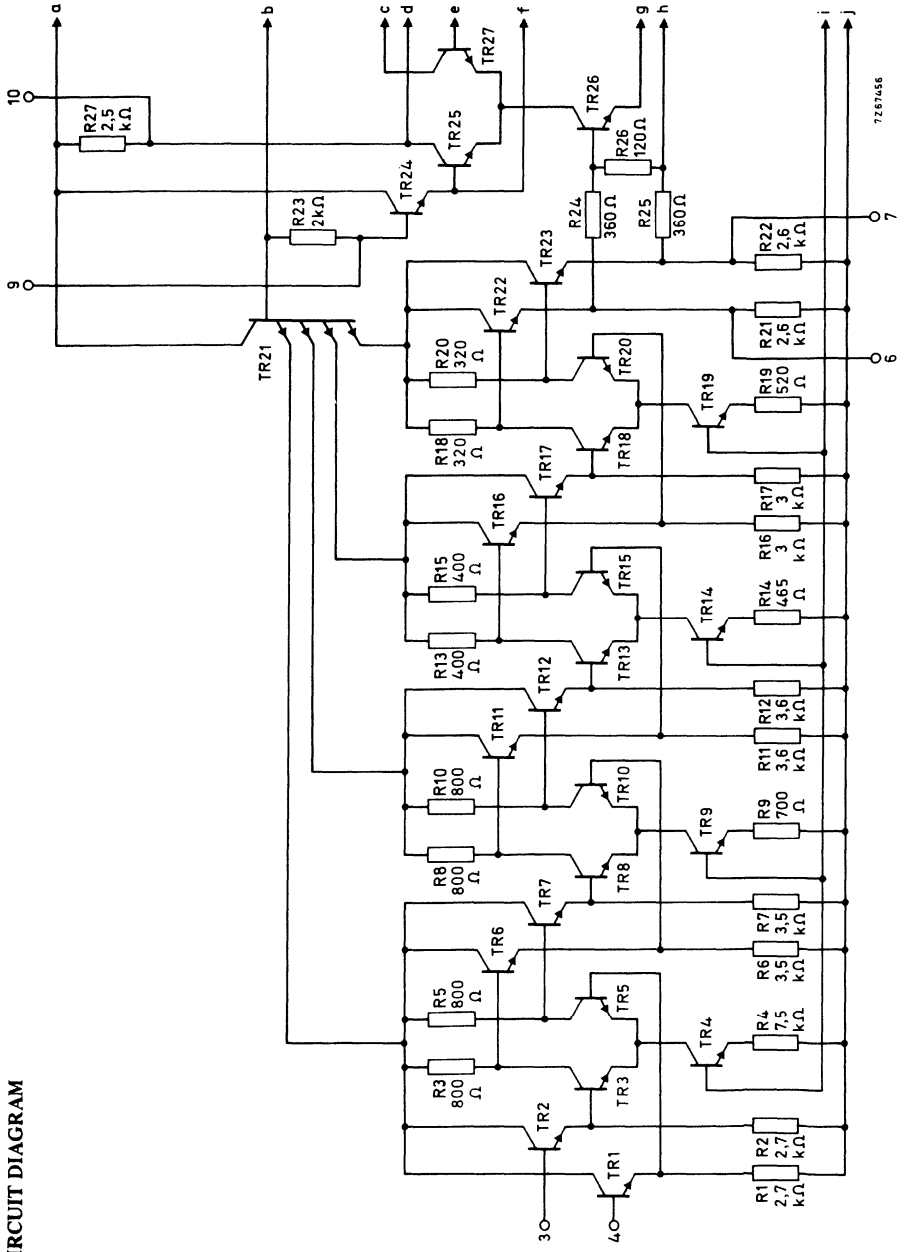
The TBA750A is a limiter-amplifier with f. m. detector, d.c. volume control and a.f. pre-amplifier. It is intended for 4,5 MHz, 5,5 MHz or 10,7 MHz.
The limiter-amplifier is a four-stage differential amplifier that gives very good noise and interference suppression.
The detector is of the balanced type. The d.c. volume control stage has excellent control characteristics with a control range of more than 80 dB.
The a.f. pre-amplifier can drive a triode-pentode output stage or a class-A push-pull transistor output stage.

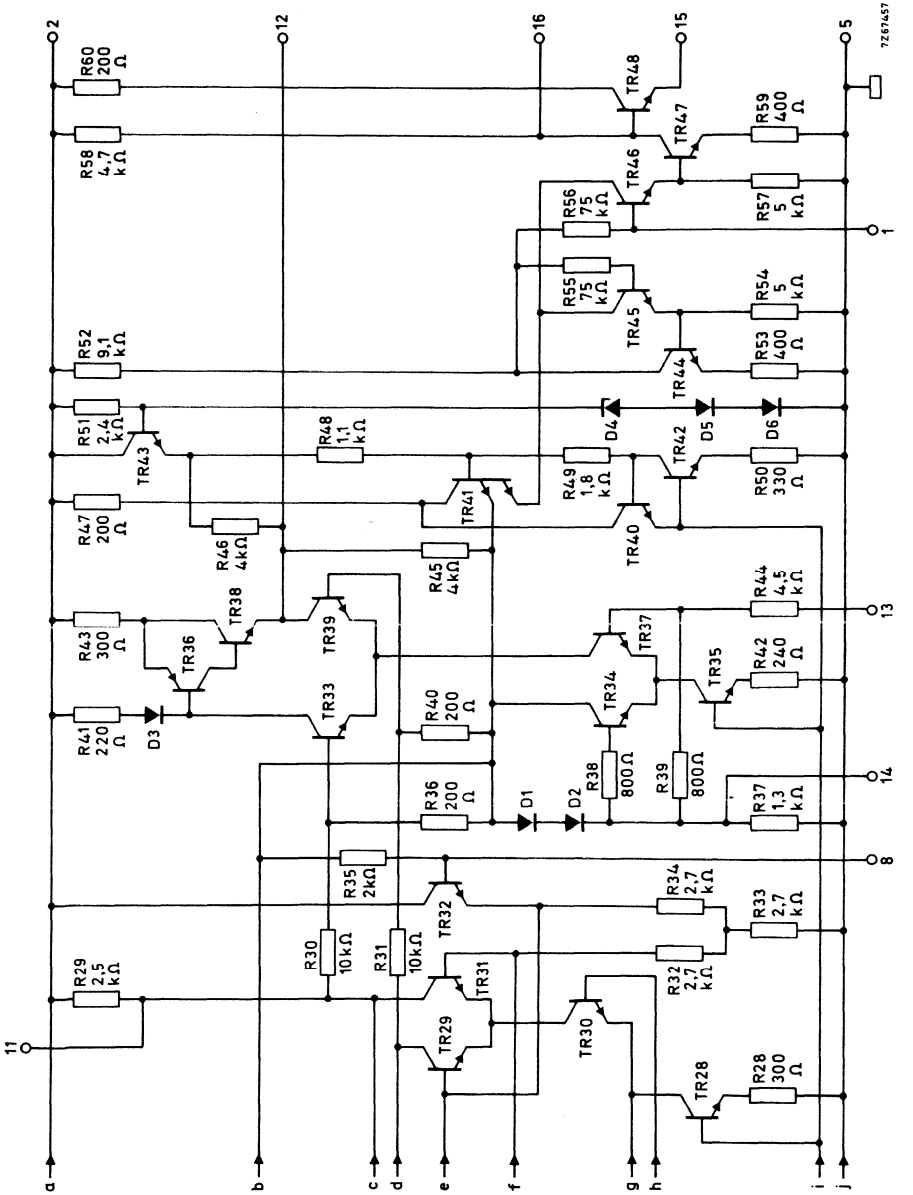
QUICK REFERENCE DATA				
Supply voltage	V_{2-5}	typ.	12	V
Total current drain	I_{tot}	typ.	30	mA
Frequency	f_o		5,5	MHz
Input voltage of start of limiting	$V_{i\,lim}$	typ.	200	μV
A.M. rejection at V_i = 1 mV	α	typ.	45	dB
A.F. output voltage at $\Delta f = \pm$ 15 kHz at pin 16	$V_{o(rms)}$	typ.	2	V
D.C. volume control range		>	80	dB

PACKAGE OUTLINE

TBA750A : 16 lead plastic dual in-line (type A) (See General Section)
TBA750AQ: 16 lead plastic quadruple in-line (See General Section)

CIRCUIT DIAGRAM

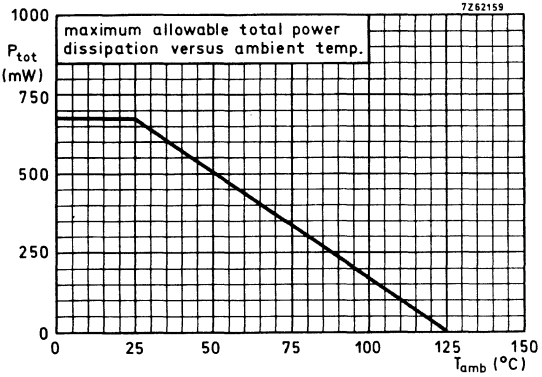



2
12
16
15
5
1
13
14
8
11
a
b
c
d
e
f
g
h
i
j
R60 200 Ω
R58 4.7 kΩ
R52 9.1 kΩ
R51 2.4 kΩ
R47 200 Ω
R43 300 Ω
R41 220 Ω
R29 2.5 kΩ
R46 4kΩ
R48 1.1 kΩ
R45 4kΩ
R40 200 Ω
R36 200 Ω
R35 2kΩ
R30 10kΩ
R31 10kΩ
R49 1.8 kΩ
R38 800Ω
R39 800Ω
R56 75 kΩ
R55 75 kΩ
R48 TR47
R59 400 Ω
R57 5 kΩ
R54 5 kΩ
R53 400 Ω
R50 330 Ω
R44 4.5 kΩ
R42 240 Ω
R37 1.3 kΩ
R34 2.7 kΩ
R33 2.7 kΩ
R32 2.7 kΩ
R28 300 Ω
TR48
TR47
TR46
TR45
TR44
TR43
TR42
TR41
TR40
TR39
TR38
TR37
TR36
TR35
TR34
TR33
TR32
TR31
TR30
TR29
TR28
D1
D2
D3
D4
D5
D6
7267457

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{2-5}	max. 16	V [1]

Power dissipation



Temperatures

Storage temperature	T_{stg}	−55 to +125	°C
Operating ambient temperature	T_{amb}	−25 to + 55	°C

CHARACTERISTICS measured in the test circuit on page 5.

Supply voltage range (See graph R_S versus supply voltage on page 6)	V_{2-5}	10 to 25	V
Total current drain	I_2	21 to 39	mA [2]
Input limiting voltage at V_o = -3 dB	$V_{i\,lim(rms)}$	typ. 200	µV
I.F. output voltage at pin 6 and 7 (peak-to-peak value)	$V_{6-5(p-p)}$ / $V_{7-5(p-p)}$	typ. 380	mV

[1]) Allowable only if the dissipation in the IC is limited by means of a series resistor in the supply. (see upper graph on page 6).

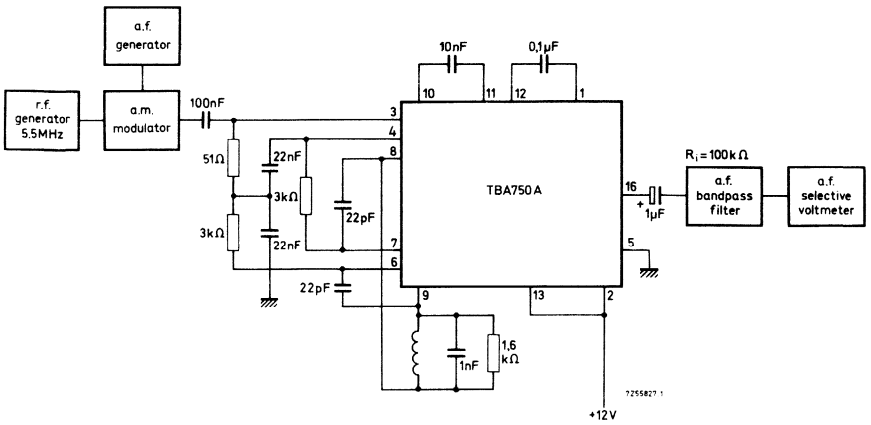
[2]) Pin 15 not connected.

CHARACTERISTICS (continued)

A.M. rejection at V_i = 1 mV	α	typ.	45	dB
V_i = 10 mV	α	typ.	50	dB
V_i = 100 mV	α	typ.	55	dB
D.C. volume control range		>	80	dB[1]
A.F. pre-amplifier voltage gain				
(pin 1 to pin 16)	G_v	typ.	10	
Input resistance at pin 1	R_i	≥	35	kΩ
A.F. output voltages				
Δf = ± 15 kHz; f_m = 1 kHz	$V_{10-5(rms)}$, $V_{11-5(rms)}$	typ.	65	mV
	$V_{12-5(rms)}$	typ.	200	mV
	$V_{16-5(rms)}$	typ.	2	V
Total harmonic distortion				
at pin 12; Δf = 15 kHz	d_{tot}	typ.	3	%
at pin 1 with respect to pin 16; $V_{o(rms)}$ = 3 V	d_{tot}	typ.	2,6	%

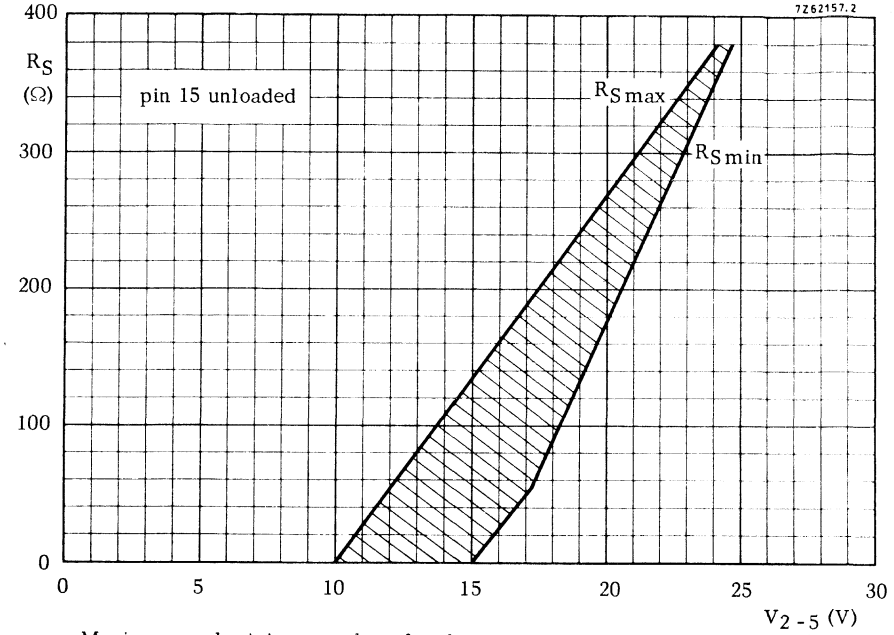
Test circuit for f.m. : f_o = 5,5 MHz; Δf = ± 15 kHz; f_m = 70 Hz

for a.m. : m = 0,3; f_m = 1 kHz

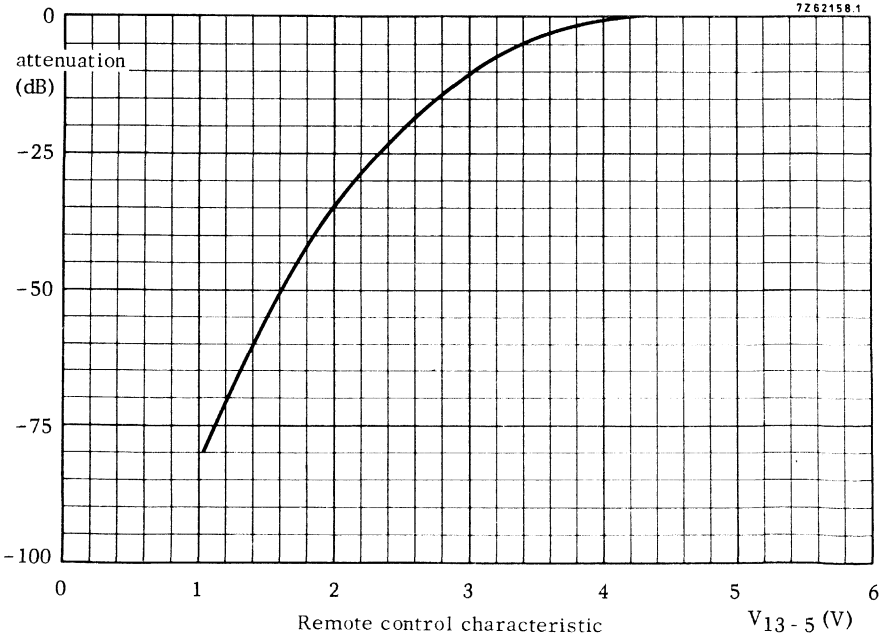


[1]) See lower graph on page 6.

CHARACTERISTICS (continued)

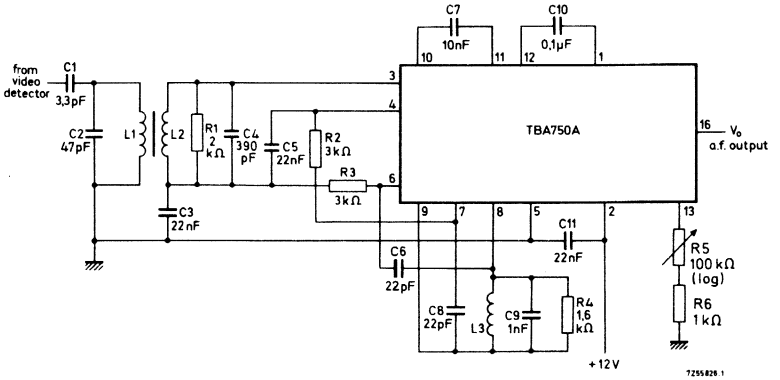


Maximum and minimum values for the power supply series resistance (R_S)



Remote control characteristic

APPLICATION INFORMATION at f = 5,5 MHz



L1 = 18 µH; Q_{L1} = 36

L2 = 2,2 µH; Q_{L2} = 21

L3 = 0,84µH; Q_{L3} = 25

Note: Q_{L1}, Q_{L2} and Q_{L3} are the loaded Q-factors.

The transfer ratio of the input bandpass filter: $\frac{V_2}{V_1}$ = 0,54

The peak-to-peak bandwidth of the detector S-curve is 300 kHz.

MICROPHONE AMPLIFIER

The TBA880 is a monolithic integrated microphone amplifier for use in telephone systems. It can be used with dynamic microphones of suitable impedance and sensitivity.

Special features are:

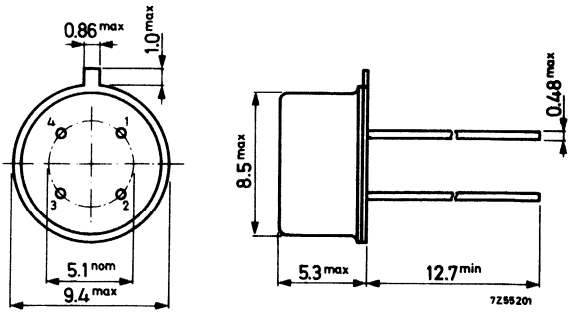
- almost constant voltage gain and d.c. voltage drop with supply current variations of 10 to 100 mA
- output voltage before limiting: 1 V (r.m.s. value)
- operation is independent of supply voltage polarity
- only one external capacitor required
- output impedance determined by internal feedback

QUICK REFERENCE DATA				
Supply current	$\pm I_2$		10 to 100	mA
Supply voltage drop	$\pm V_{1-2}$	typ.	4,8	V
Voltage gain	G_V	typ.	210	
Output impedance	R_o	typ.	100	Ω

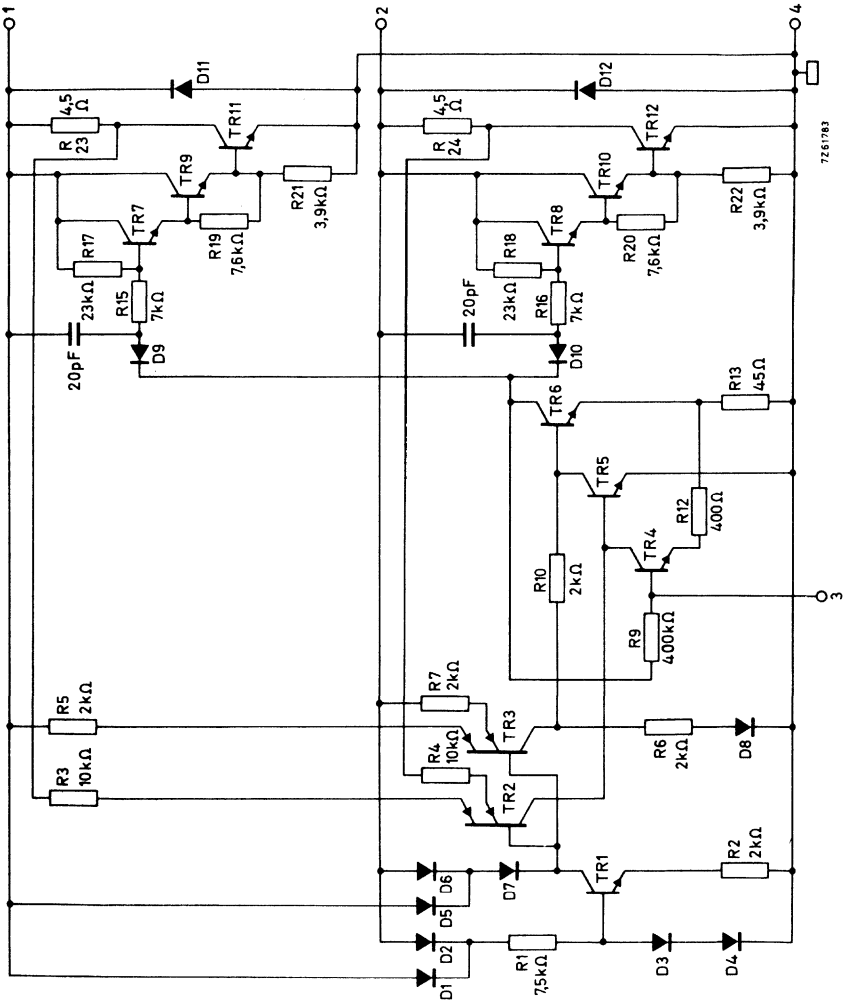
PACKAGE OUTLINE

Dimensions in mm

TO-12



CIRCUIT DIAGRAM



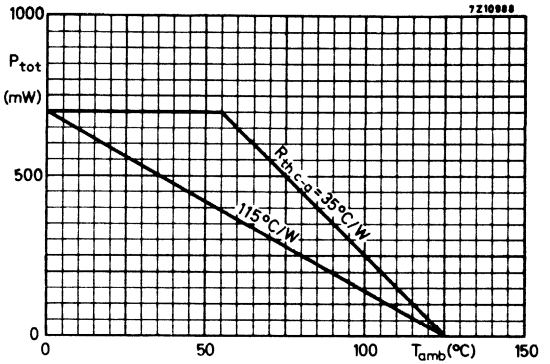
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Currents

Supply current (d.c.)	I_2	−100 to +100		mA
A.C. component of supply current (peak value)	I_{2m}	max.	100	mA
Pin No. 3 current	I_3	max.	100	μA

Power dissipation

Total power dissipation	P_{tot}	max.	700	mW



Temperatures

Storage temperature	T_{stg}	−55 to +125		°C
Operating ambient temperature	T_{amb}	−35 to + 75		°C

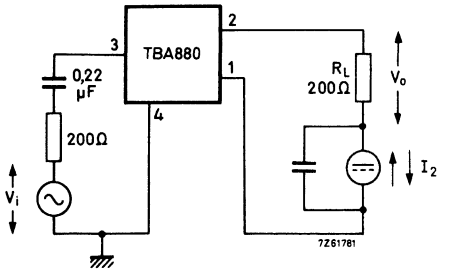
THERMAL RESISTANCE

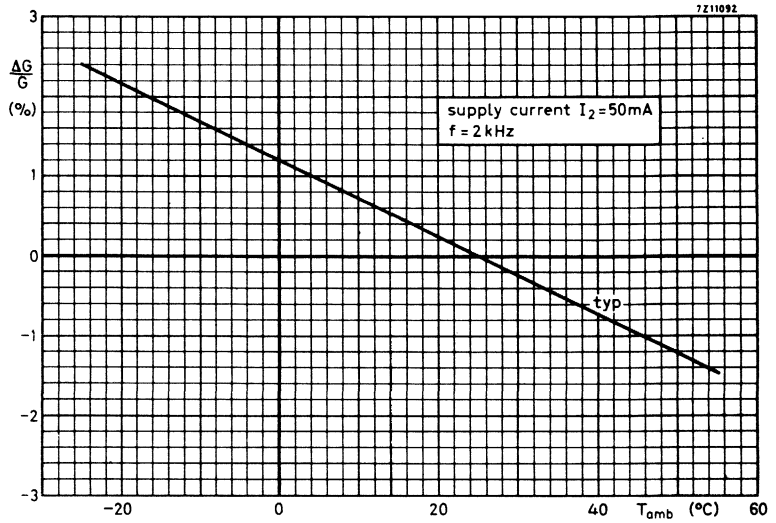
From junction to case	$R_{th\,j-c}$	=	65	°C/W

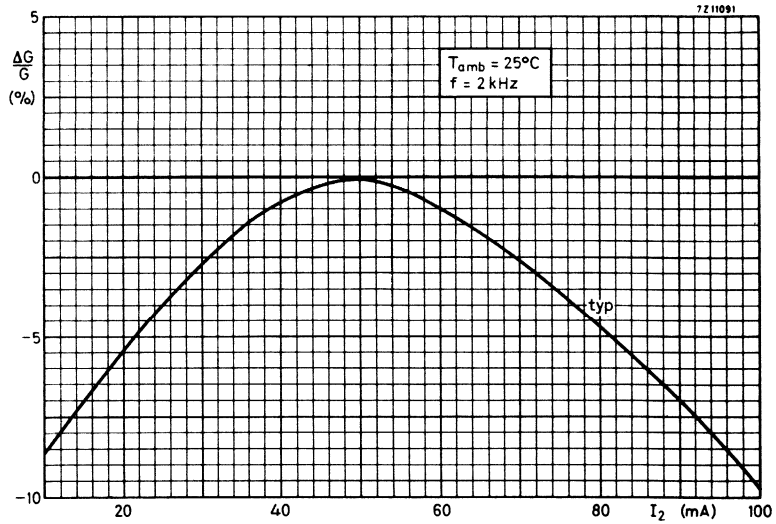
CHARACTERISTICS at R_L = 200 Ω; f = 2 kHz; T_{amb} = 25 °C unless otherwise specified. (see test circuit below).

Supply voltage drop at $R_{th\ j\text{-}a}$ = 100 °C/W				
± I_2 = 10 mA	$\pm V_{1\text{-}2}$	typ. <	4,5 5,4	V V
± I_2 = 50 mA	$\pm V_{1\text{-}2}$	<	5,8	V
± I_2 = 100 mA	$\pm V_{1\text{-}2}$	<	6,0	V
Voltage gain				
± I_2 = 10 mA	G_v	typ.	200	
± I_2 = 50 mA	G_v	typ.	210	
Change of voltage gain due to change of supply voltage polarity	ΔG_v	<	10	%
Gain reduction at f = 300 Hz (with respect to f = 2 kHz)	ΔG_v	typ. <	1 3	dB dB
Output impedance at ± I_2 = 50 mA	R_o	typ.	100	Ω
Noise output voltage at B = 0,3 kHz to 4 kHz	$V_{n(rms)}$	typ.	1,0	mV
Output voltage				
I_2 = 25 mA; d_{tot} = 5%	$V_{o(rms)}$	> typ.	0,85 1,0	V V

Test circuit:




7Z11092
3
ΔG/G (%)
1
0
-1
-2
-3
supply current I_2=50mA
f = 2 kHz
typ
-20
0
20
40
T_{amb} (°C)
60


7Z11091
5
ΔG/G (%)
0
-5
-10
T_{amb} = 25°C
f = 2 kHz
typ
20
40
60
80
I_2 (mA)
100

TELEVISION SIGNAL PROCESSING CIRCUIT

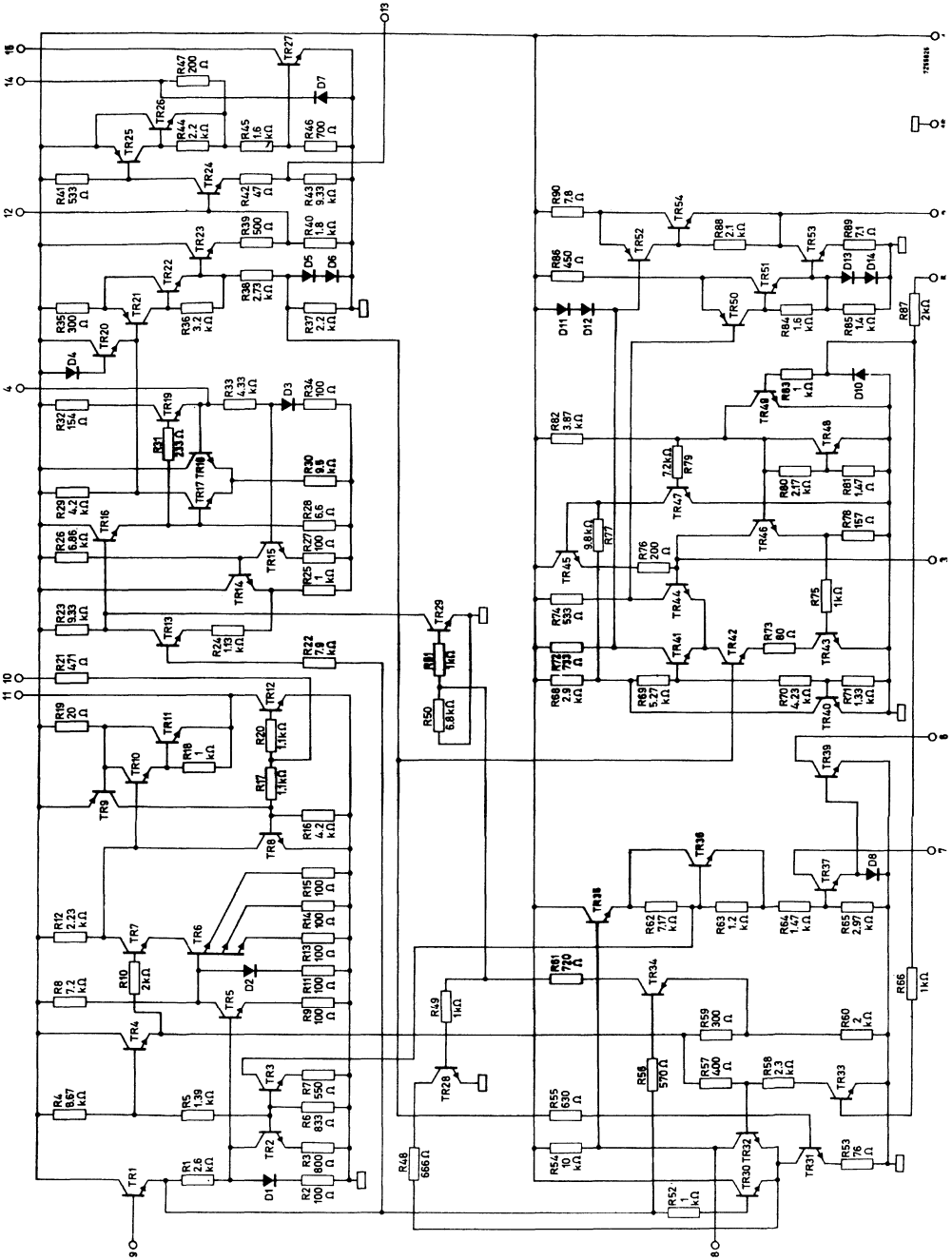
The TBA890 is a silicon monolithic integrated signal processing circuit for monochrome and colour television receivers.
It combines the following functions:
- video pre-amplifier with emitter-follower output and short circuit protection.
- blanking facility for the video amplifier.
- gated a.g.c. detector supplying the a.g.c. voltages for the vision i.f. amplifier and tuner.
- noise cancelling circuit in the a.g.c. and sync. separator circuits.
- sync. separator.
- automatic horizontal phase detector
- vertical sync. pulse separator.

The circuit is designed for receivers equipped with tubes or transistors in the deflection and video output stages.
The control stages in the i.f. amplifier and the tuner have to be equipped with n-p-n transistors. The equivalent circuit for tuners equipped with a p-n-p transistor is the TBA900. The circuit is developed for signals with negative modulation.

QUICK REFERENCE DATA				
Supply voltage	V_P	typ.	12	V
Ambient temperature	T_{amb}	typ.	25	°C
Video input voltage (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	2.7	V
Voltage gain of the video amplifier	G_v	typ.	7	dB
A.G.C. voltage for i.f. part	V_{7-16}	1.0 to	12	V
A.G.C. voltage for tuner	V_{6-16}	0.3 to	12	V
Output voltage range horizontal phase detector	V_{2-16}	2 to	10	V
Vertical sync. output voltage (positive going pulse; peak-to-peak value)	$V_{14-16(p-p)}$	typ.	11	V

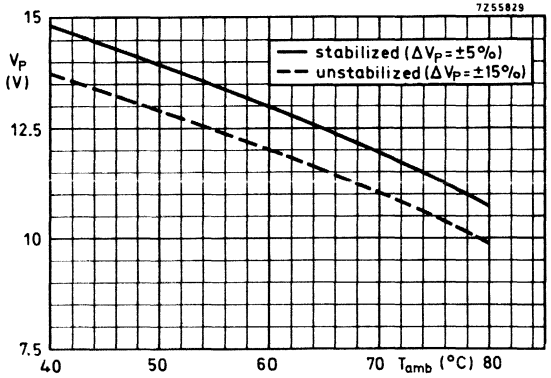
PACKAGE OUTLINE

TBA890 : 16 lead plastic dual in-line (type A) (See General Section)
TBA890Q: 16 lead plastic quadruple in-line (See General Section)



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.		20	V[1]
Power dissipation	P_{tot}	max.		700	mW
Temperatures					
Storage temperature	T_{stg}	-55	to	+125	°C
Operating ambient temperature	T_{amb}	-25	to	+80	°C



Maximum allowable nominal supply voltage as a function of the maximum ambient temperature.

[1] Allowed only while receiver is warming up.

CHARACTERISTICS

Supply voltage range V_P See curves on page 3

The following characteristics are measured in the circuit on p. 7 at T_{amb} = 25 °C; V_P = 12 V.

Video amplifier

Input resistance	R_{9-16}	>	30	kΩ
Input capacitance	C_{9-16}	<	3	pF
Bandwidth (3 dB)	B	>	5	MHz
Linearity (m)		>	0.9	
Rise time and fall time at the output	t_r; t_f	<	50	ns
Voltage gain	G_v	typ.	7	dB
Video input voltage (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	2.7	V 1)
D.C. bias video detector voltage	V_{bias}	typ.	6	V 2)
Video output voltage (peak-to-peak value)	$V_{11-16(p-p)}$	typ.	6	V 1)
Black level at the output	V_{11-16}	typ.	5	V 3)
Available video output current (peak value)	I_{11M}	≤	30	mA 4)

Tolerances on the video output voltages

I.C. processing spreads	$\pm\Delta V_{11-16}$	<	420	mV 5)
Temperature drift	$-\Delta V_{11-16}$	typ.	1.8	mV/°C
Spreads over a.g.c. expansion (entire range)	$\pm\Delta V_{11-16}$	<	100	mV 6)
Supply voltage	$\frac{\Delta V_{11-16}}{\Delta V_P}$	typ.	0.5	

1) Signal with negative going sync.; this value is obtained only when the input signal meets the C.C.I.R. standard.

2) A voltage divider with 5% tolerance resistors is required between pin 9 and supply terminal.

3) Only valid if the video signal is in accordance with the C.C.I.R. standard.

4) The total load on pin 11 must be such that the d.c. output current $I_{11} \leq 15$ mA.

5) The spreads of the voltage divider for the bias of the video detector of ± 5% is included in this figure.

6) Variation about a nominal condition, the i.f. being fully controlled and the tuner uncontrolled.

CHARACTERISTICS (continued)

Tolerances on the black level at the output				
I.C. processing spreads	$\pm\Delta V_{11\text{-}16}$	<	420	mV[1]
Temperature drift	$-\Delta V_{11\text{-}16}$	typ.	1.7	mV/°C
Spreads over a.g.c. expansion (entire range)	$\pm\Delta V_{11\text{-}16}$	<	130	mV[2]
Supply voltage	$\frac{\Delta V_{11\text{-}16}}{\Delta V_P}$	typ.	0.4	
Video blanking				
Input voltage (peak-to-peak value)	$V_{10\text{-}16(p\text{-}p)}$		1 to 5	V
Input resistance	$R_{10\text{-}16}$	typ.	1	kΩ
Output voltage during blanking	$V_{11\text{-}16}$	<	500	mV
A.G.C. circuit				
Range of control voltage i.f. amplifier	$V_{7\text{-}16}$		1 to 12	V[3]
Range of control voltage tuner	$V_{6\text{-}16}$		0.3 to 12	V[3]
Signal expansion for full control of i.f. amplifier and tuner		typ.	0.5	dB
Current i.f. control point	I_7	<	20	mA
Current tuner control point	I_6	<	20	mA
Current i.f. control point for tuner take-over	I_7	see note 4		
Keying input pulse (peak-to-peak value)	$V_{5\text{-}16(p\text{-}p)}$	see note 5		
Input resistance	$R_{5\text{-}16}$	typ.	2	kΩ

1) The spreads of the voltage divider for the bias of the video detector of ± 5% is included in this figure (pin 9).

2) Variation about a nominal condition, the i.f. being fully controlled and the tuner uncontrolled.

3) Positive going at increasing input signal.

4) This value depends on the ratio between the external impedances on pins 6 and 7. With equal impedances the current of the i.f. control point at tuner take-over will be about 16% from its maximum value (minimum control voltage).

5) Negative going pulse is required. The voltage during scan should be between 1 V and 2 V.

CHARACTERISTICS (continued)

Horizontal synchronization circuit				
Sync. separator			see note 1	
Output voltage range of phase detector	V_{2-16}		2 to 10	V [2]
Control steepness	S_φ	typ.	2.5	V/μs [3]
Phase deviation between front edge sync. pulse and front edge flyback pulse	φ_0	typ.	1.5	μs
Variation φ_0 caused by internal spreads	$\pm\Delta_{\varphi 0}$	typ.	0.3	μs [4]
Output voltage range as a frequency detector	V_{2-16}		4 to 8	V [5]
Vertical synchronization circuit				
Output voltage vertical sync. pulse generator	V_{14-16}	typ.	11	V
Output impedance	R_{14-16}	typ.	2	kΩ

1) The sync. pulse is sliced about 25% below top sync. level. A sliding bias circuit makes the slicing level independent of the signal strength.

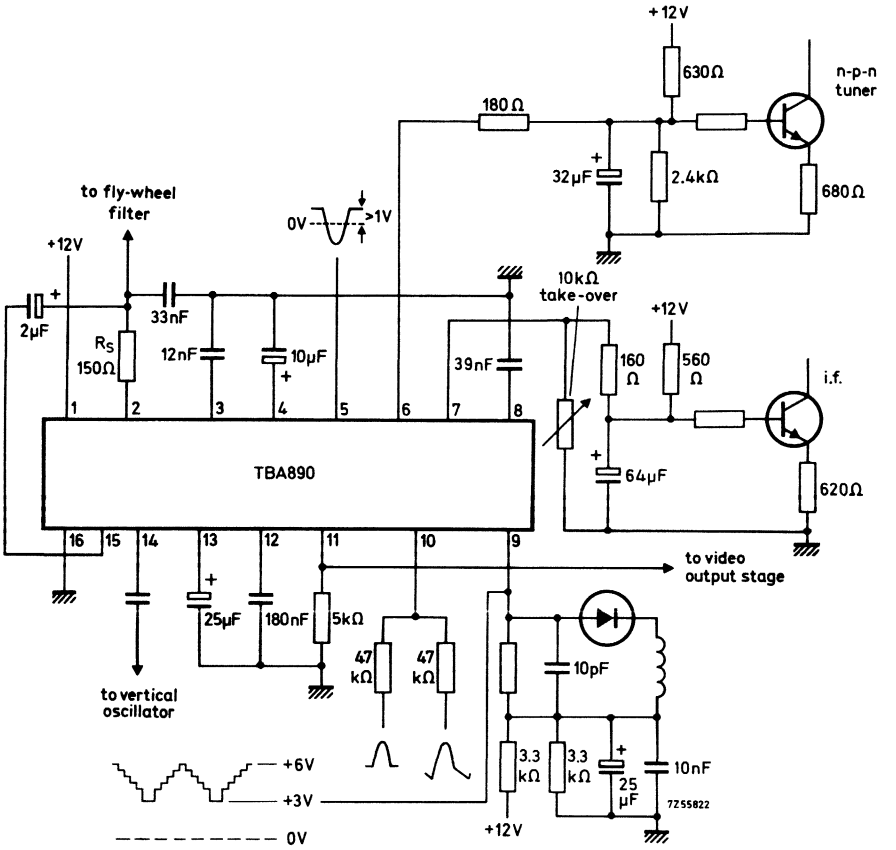
2) Nominal voltage 6 V.

3) Higher values of this control steepness can be obtained by changing R_S (see circuit on page 7). For example R_S = 56 Ω, S_φ = 5 V/μs and R_S = 0, S_φ = ≥25 V/μs.

4) In addition to this figure ± 7% of the retrace time of the sawtooth generated on pin 3 has to be added to find the total spreads of φ_0.
This value of ± 7% is obtained only when the tolerance of the capacitor connected to pin 3 does not exceed ± 10%.

5) Nominal voltage 6 V.
The load impedance on pin 2 of the circuit on page 7 is about 50 kΩ.
When a higher impedance is used (tube equipped reactance stage) values from 2 V to 10 V can be reached.

APPLICATION INFORMATION



TELEVISION SIGNAL PROCESSING CIRCUIT

The TBA900 is a silicon monolithic integrated signal processing circuit for monochrome and colour television receivers.

It combines the following functions:

- video pre-amplifier with emitter-follower output and short circuit protection.
- blanking facility for the video amplifier.
- gated a.g.c. detector supplying the a.g.c. voltages for the vision i.f. amplifier and tuner.
- noise cancelling circuit in the a.g.c. and sync. separator circuits.
- sync. separator.
- automatic horizontal phase detector
- vertical sync. pulse separator.

The circuit is designed for receivers equipped with tubes or transistors in the deflection and video output stages.

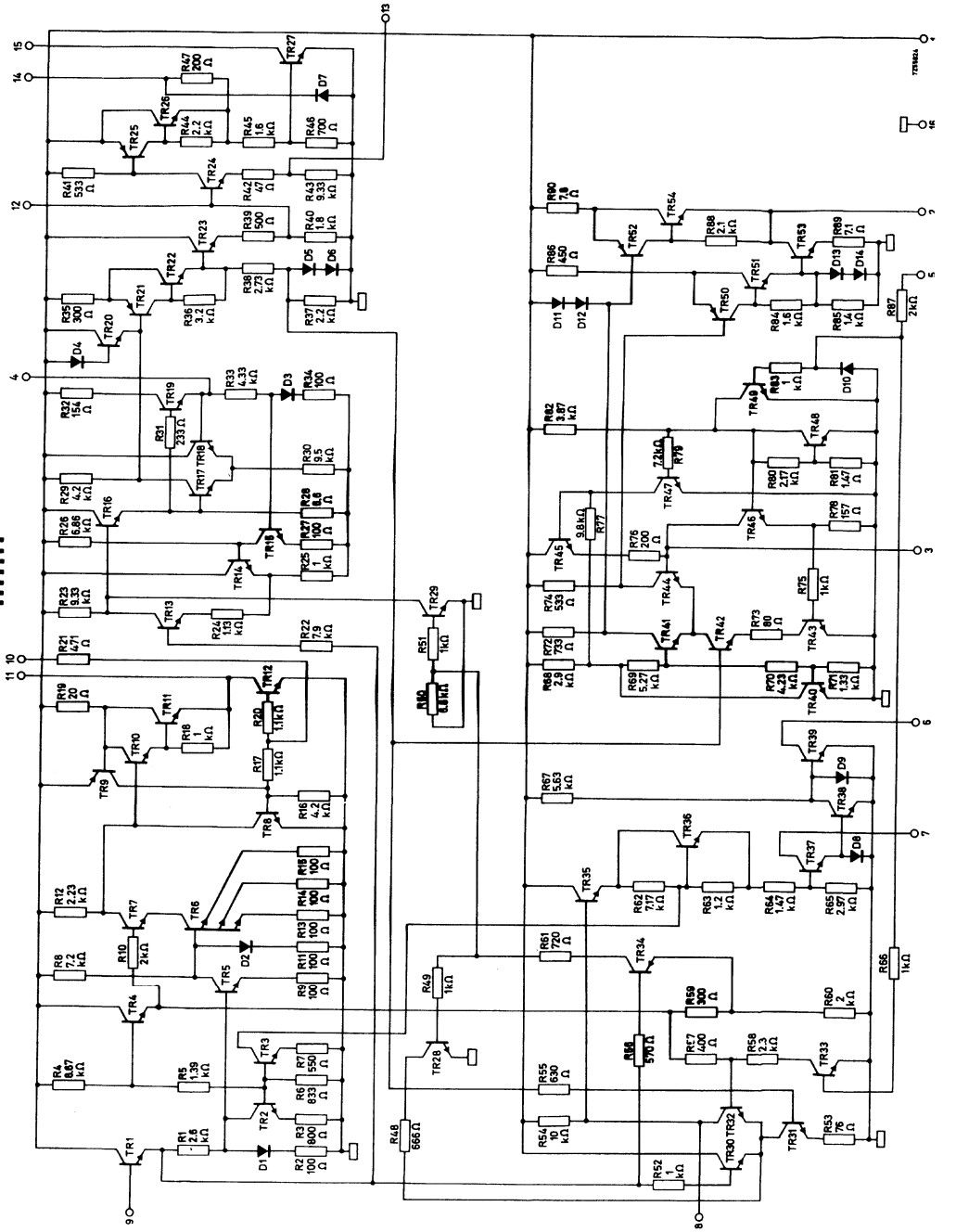
The control stage in the i.f. amplifier has to be equipped with an n-p-n transistor and the tuner with a p-n-p transistor.

The circuit is developed for signals with negative modulation.

QUICK REFERENCE DATA				
Supply voltage	V_P	typ.	12	V
Ambient temperature	T_{amb}	typ.	25	°C
Video input voltage (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	2.7	V
Voltage gain of the video amplifier	G_v	typ.	7	dB
A.G.C. voltage for i.f. part	V_{7-16}	1.0 to	12	V
A.G.C. voltage for tuner	V_{6-16}	0.3 to	12	V
Output voltage range horizontal phase detector	V_{2-16}	2 to	10	V
Vertical sync. output voltage (positive going pulse; peak-to-peak value)	$V_{14-16(p-p)}$	typ.	11	V

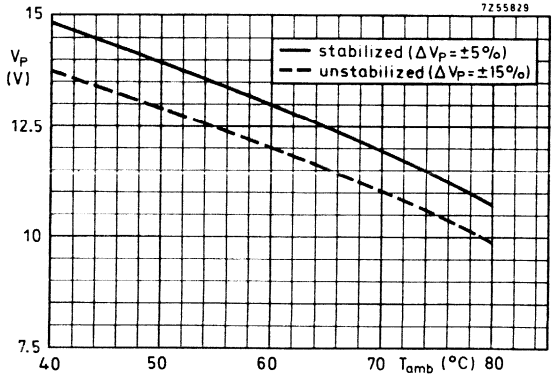
PACKAGE OUTLINE

TBA900 : 16 lead plastic dual in-line (type A) (See General Section)
TBA900Q: 16 lead plastic quadruple in-line (See General Section)



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.		20	V [1]
Power dissipation	P_{tot}	max.		700	mW
Temperatures					
Storage temperature	T_{stg}	−55	to	+125	°C
Operating ambient temperature	T_{amb}	-25	to	+80	°C



Maximum allowable nominal supply voltage as a function of the maximum ambient temperature.

[1] Allowed only while receiver is warming up.

CHARACTERISTICS

Supply voltage range	V_P	See curves on page 3		

The following characteristics are measured in the circuit on p. 7 at T_{amb} = 25 °C; V_P = 12 V.

Video amplifier				
Input resistance	R_{9-16}	>	30	kΩ
Input capacitance	C_{9-16}	<	3	pF
Bandwidth (3 dB)	B	>	5	MHz
Linearity (m)		>	0.9	
Rise time and fall time at the output	t_r; t_f	<	50	ns
Voltage gain	G_v	typ.	7	dB
Video input voltage (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	2.7	V [1]
D.C. bias video detector voltage	V_{bias}	typ.	6	V [2]
Video output voltage (peak-to-peak value)	$V_{11-16(p-p)}$	typ.	6	V [1]
Black level at the output	V_{11-16}	typ.	5	V [3]
Available video output current (peak value)	I_{11M}	≤	30	mA [4]
Tolerances on the video output voltages				
I.C. processing spreads	$\pm\Delta V_{11-16}$	<	420	mV [5]
Temperature drift	$-\Delta V_{11-16}$	typ.	1.8	mV/°C
Spreads over a.g.c. expansion (entire range)	$\pm\Delta V_{11-16}$	<	100	mV [6]
Supply voltage	$\frac{\Delta V_{11-16}}{\Delta V_P}$	typ.	0.5	

1) Signal with negative going sync.; this value is obtained only when the input signal meets the C.C.I.R. standard.

2) A voltage divider with 5% tolerance resistors is required between pin 9 and supply terminal.

3) Only valid if the video signal is in accordance with the C.C.I.R. standard.

4) The total load on pin 11 must be such that the d.c. output current $I_{11} \leq 15$ mA.

5) The spreads of the voltage divider for the bias of the video detector of ± 5% is included in this figure.

6) Variation about a nominal condition, the i.f. being fully controlled and the tuner uncontrolled.

CHARACTERISTICS (continued)

Tolerances on the black level at the output

I.C. processing spreads	$\pm\Delta V_{11\text{-}16}$	<	420	mV[1]
Temperature drift	$-\Delta V_{11\text{-}16}$	typ.	1.7	mV/°C
Spreads over a.g.c. expansion (entire range)	$\pm\Delta V_{11\text{-}16}$	<	130	mV[2]
Supply voltage	$\frac{\Delta V_{11\text{-}16}}{\Delta V_P}$	typ.	0.4	

Video blanking

Input voltage (peak-to-peak value)	$V_{10\text{-}16(p\text{-}p)}$		1 to 5	V
Input resistance	$R_{10\text{-}16}$	typ.	1	kΩ
Output voltage during blanking	$V_{11\text{-}16}$	<	500	mV

A.G.C. circuit

Range of control voltage i.f. amplifier	$V_{7\text{-}16}$		1 to 12	V[3]
Range of control voltage tuner	$V_{6\text{-}16}$		0.3 to 12	V[4]
Signal expansion for full control of i.f. amplifier and tuner		typ.	0.5	dB
Current i.f. control point	I_7	<	20	mA
Current tuner control point	I_6	<	8	mA
Current i.f. control point for tuner take-over	I_7	typ.	2	mA
Keying input pulse (peak-to-peak value)	$V_{5\text{-}16(p\text{-}p)}$	see note 5		
Input resistance	$R_{5\text{-}16}$	typ.	2	kΩ

1) The spreads of the voltage divider for the bias of the video detector of ± 5% is included in this figure (pin 9).

2) Variation about a nominal condition, the i.f. being fully controlled and the tuner uncontrolled.

3) Positive going at increasing input signal.

4) Negative going at increasing input signal.

5) Negative going pulse is required. The voltage during scan should be between 1 V and 2 V.

CHARACTERISTICS (continued)

Horizontal synchronization circuit				
Sync. separator			see note 1	
Output voltage range of phase detector	V_{2-16}		2 to 10	V [2]
Control steepness	S_φ	typ.	2.5	V/μs [3]
Phase deviation between front edge sync. pulse and front edge flyback pulse	φ_0	typ.	1.5	μs
Variation φ_0 caused by internal spreads	$\pm\Delta_{\varphi 0}$	typ.	0.3	μs [4]
Output voltage range as a frequency detector	V_{2-16}		4 to 8	V [5]
Vertical synchronization circuit				
Output voltage vertical sync. pulse generator	V_{14-16}	typ.	11	V
Output impedance	R_{14-16}	typ.	2	kΩ

1) The sync. pulse is sliced about 25% below top sync. level. A sliding bias circuit makes the slicing level independent of the signal strength.

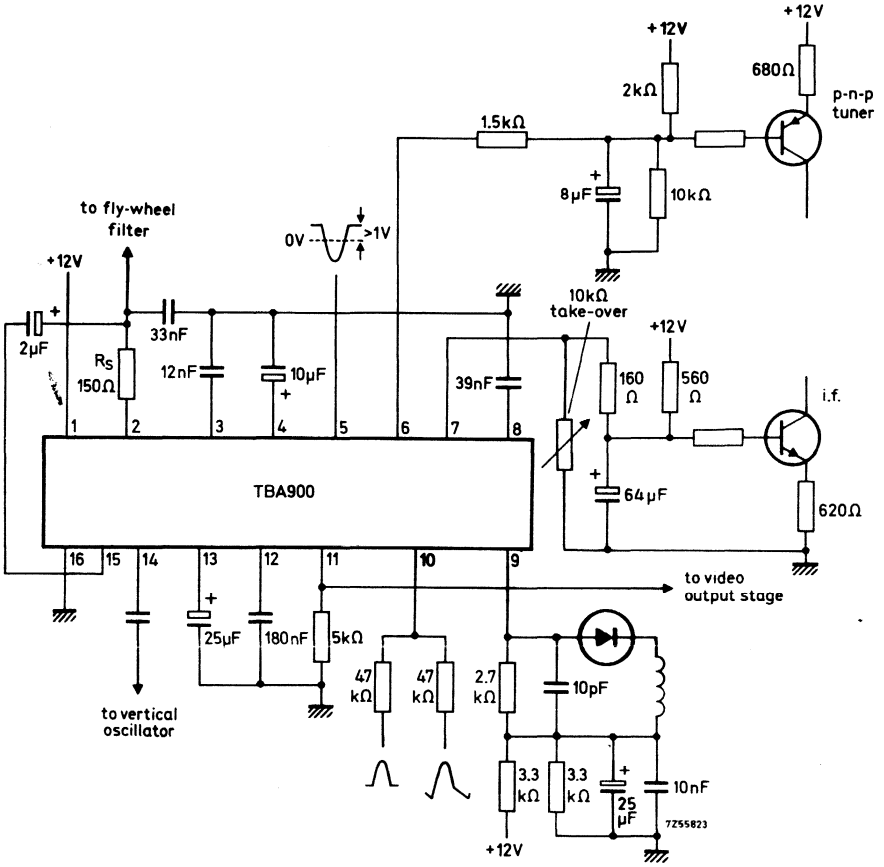
2) Nominal voltage 6 V.

3) Higher values of this control steepness can be obtained by changing R_S (see circuit on page 7). For example R_S = 56 Ω, S_φ = 5 V/μs and R_S = 0, S_φ = ≥25 V/μs.

4) In addition to this figure ± 7% of the retrace time of the sawtooth generated on pin 3 has to be added to find the total spreads of φ_0.
This value of ± 7% is obtained only when the tolerance of the capacitor connected to pin 3 does not exceed ± 10%.

5) Nominal voltage 6 V.
The load impedance on pin 2 of the circuit on page 7 is about 50 kΩ.
When a higher impedance is used (tube equipped reactance stage) values from 2 V to 10 V can be reached.

APPLICATION INFORMATION



AUDIO AMPLIFIER

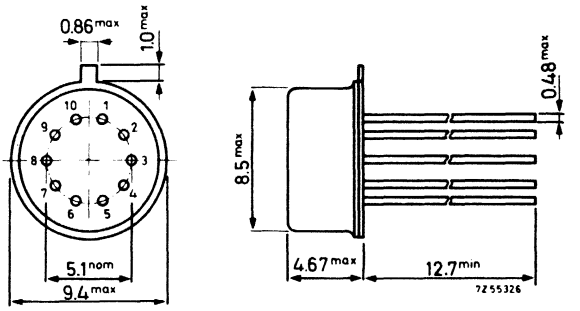
The TBA915 is a monolithic integrated a.f. amplifier designed for use in small communication receivers, where low battery drain is of paramount importance.
The output power of the device is 500 mW and the zero-signal current is only 2 mA (typ.).
The circuit can be squelched to a stand-by current of 0,4 mA.

QUICK REFERENCE DATA				
Supply voltage	V_P	nom.	12	V
Output power at R_L = 20 Ω	P_o	typ.	500	mW
Input signal for P_o = 500 mW	V_i	typ.	10	mV
Input impedance	R_i	typ.	9	kΩ
Total current (no signal)	I_{tot}	typ.	2	mA
(squelched)	I_{tot}	typ.	0,4	mA

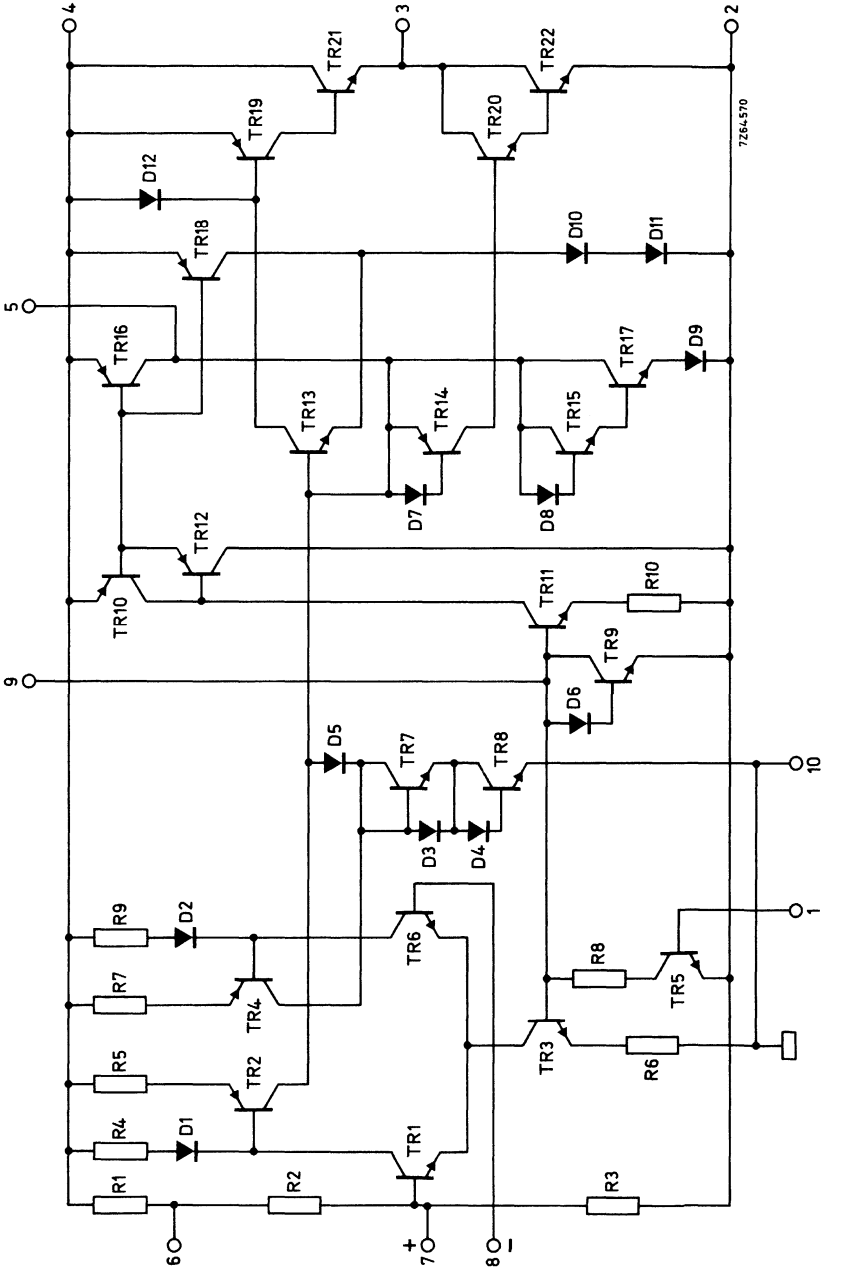
PACKAGE OUTLINE

Dimensions in mm

TO-74 (reduced height)



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134).

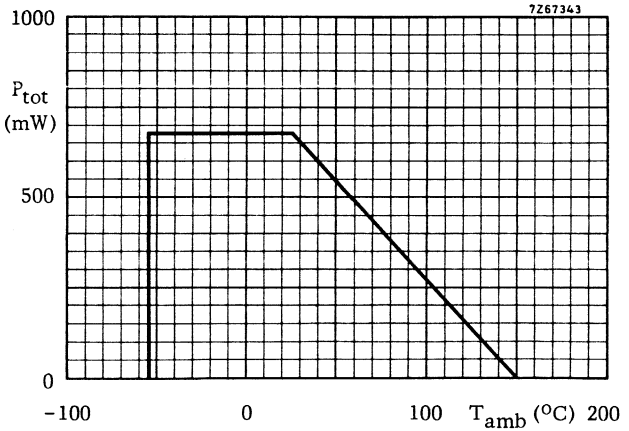
Voltages (pin 2 must be externally connected to pin 10)

Pin No. 4 voltage	V_{4-2}	max.	17	V
Pin No. 8 voltage	$\pm V_{8-7}$	max.	5	V
Pin No. 3 voltage	V_{3-2}	max.	17	V

Currents

Pin No. 4 current	I_4	max.	350	mA
Pin No. 3 current	$\pm I_3$	max.	350	mA
Pin No. 7 current	I_7	max.	0,5	mA
Pin No. 8 current	I_8	max.	0,5	mA
Pin No. 5 current	I_5	max.	5	mA
Pin No. 9 current	I_9	max.	5	mA
Pin No. 1 current	$+I_1$	max.	1	mA
	$-I_1$	max.	10	μA

Total power dissipation



Temperatures

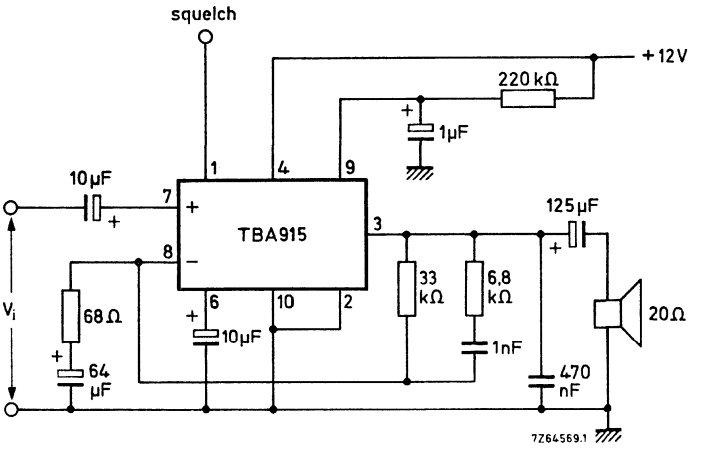
Storage temperature	T_{stg}	−55 to +125	°C
Operating ambient temperature see derating curve above	T_{amb}	−55 to +125	°C

CHARACTERISTICS at T_{amb} = 25 °C; V_P = 12 V

Measured in the test circuit below

Output power at d_{tot} = 5%	P_o	typ.	500	mW
Bandwidth (−3 dB)	B	>	6	kHz
Total current (d.c.)				
no signal	I_{tot}	typ.	2	mA
		<	3,5	mA
no signal with squelch	I_{tot}	typ.	0,4	mA
with signal at P_o = 500 mW	I_{tot}	typ.	72	mA
Total distortion at P_o = 500 mW	d_{tot}	typ.	2,5	%
		<	5	%
Input signal at P_o = 500 mW	V_i	typ.	10	mV
		<	15	mV
Input impedance	$\|Z_i\|$	typ.	9	kΩ
Signal to noise ratio				
related to P_o = 500 mW R_S = 600 Ω; B = 300 Hz to 6 kHz	$\frac{S}{N}$	typ.	72	dB
Bias current	I_9	>	25	μA

Test circuit



SQUELCH REQUIREMENTS at I_9 = 25 to 75 μA

Squelch "on"	V_1	>	800	mV
	I_1	>	10	μA
Squelch "off"	V_1	<	400	mV

HORIZONTAL COMBINATION

The TBA920 is a monolithic integrated circuit intended for television receivers with transistor-thyristor-or tube equipped output stages.
It combines the following functions:
- noise gated sync separator
- line oscillator
- phase comparison between sync pulse and oscillator
- loopgain and time constant switching (also for video recorder applications)
- phase comparison between line-flyback pulse and oscillator
- output stage for drive a variety of line output stages

QUICK REFERENCE DATA				
Supply voltage	V_{1-16}	nom.	12	V
Ambient temperature	T_{amb}		25	°C
Input signals				
Video input voltage (positive going sync)	$V_{8-16(p-p)}$	typ.	3	V
top sync to white value			1 to 7	V
Noise gate input current (peak value)	I_{9M}	>	30	µA
Input resistance of noise gate	R_{9-16}	typ.	200	Ω
Flyback signal input voltage (peak value)	V_{5-16M}	typ.	±1	V
Flyback signal input current (peak value)	I_{5M}	typ.	1	mA
Output signals				
Line driver output voltage (peak-to-peak value)	$V_{2-16(p-p)}$	typ.	10	V
Line driver output current (average value)	$I_{2(AV)}$	max.	20	mA
Line driver output current (peak value)	I_{2M}	max.	200	mA
Composite sync output voltage (peak value)	V_{7-16M}	typ.	10	V

PACKAGE OUTLINE TBA920 : 16 lead plastic dual in-line (See General Section)
TBA920Q: 16 lead plastic quadruple in-line (See General Section)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages				
Supply voltage	V_{1-16}	max.	13,2	V
Pin No. 3 voltage	V_{3-16}		0 to 13,2	V
Pin No. 8 voltage	$-V_{8-16}$	max.	12	V
Pin No. 10 voltage	V_{10-16}		−0,5 to +5	V
Currents				
Pin No. 2 current (average value)	$I_{2(AV)}$	max.	20	mA
(peak value)	I_{2M}	max.	200	mA
Pin No. 5 current (peak value)	I_{5M}	max.	10	mA
Pin No. 7 current (peak value)	I_{7M}	max.	10	mA
Pin No. 8 current (peak value)	I_{8M}	max.	10	mA
Pin No. 9 current (peak value)	I_{9M}	max.	10	mA
Power dissipation				
Total power dissipation	P_{tot}	max.	600	mW [1]
Temperatures				
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		−20 to +60	°C

CHARACTERISTICS at V_{1-16} = 12 V; T_{amb} = 25 °C

Measured in circuit on page 6 (CCIR standard).

Current consumption at I_2 = 0	I_1	typ.	36	mA
Required input signals				
Video signal				
Input voltage (positive going sync) peak-to-peak value	$V_{i(p-p)}$	typ.	3	V
			1 to 7	V
Input current during sync pulse (peak value)	I_{8M}	typ.	100	μA
Noise gating (pin 9)				
Input voltage (peak value)	V_{9-16M}	>	0,7	V
Input current (peak value)	I_{9M}	>	30	μA
		<	10	mA
Input resistance	R_{9-16}	typ.	200	Ω

1) 800 mW permissible while tubes are heating up.

CHARACTERISTICS (continued)

Flyback pulse (pin 5)

Input voltage (peak value)	V_{5-16M}	typ.	±1	V	
Input current (peak value)	I_{5M}	>	50	μA	
		typ.	1	mA	
Input resistance	R_{5-16}	typ.	400	Ω	
Pulse duration at 15625 Hz	t_5	>	10	μs	

Delivered output signals

Composite sync pulses (positive; pin 7)

Output voltage (peak-to-peak value)	$V_{7-16(p-p)}$	typ.	10	V	
Output resistance					
at leading edge of pulse (emitter follower)	R_{7-16}	≈	50	Ω	
at trailing edge	R_{7-16}	typ.	2,2	kΩ	
Additional external load resistance	$R_{7-16(ext)}$	>	2	kΩ	

Driver pulse (pin 2)

Output voltage (peak-to-peak value)	$V_{2-16(p-p)}$	typ.	10	V	
Average output current	$I_{2(AV)}$	<	20	mA	
Peak output current	I_{2M}	<	200	mA	
Output resistance (low ohmic)	R_{2-16}	typ.	2,5 or 15	Ω	[1]
Output pulse duration when synchronised	t_2		12 to 32	μs	[2]
Permissible delay between leading edge of output pulse and flyback pulse at t_5 = 12 μs	$t_{o\ tot}$		0 to 15	μs	
Supply voltage at which output pulses are obtained	V_{1-16}	>	4	V	

[1]) Depends on switch position and polarity output current. R_{2-16} = 2,5 Ω is valid for V_{2-16} = +10,5 V and a load between pins 2 and 16 (e.g. an external resistor).

[2]) The output pulse duration is adjusted by shifting the leading edge (V_{3-16} from 6 V to 8 V). The pulse duration is a result of delay in the line output device and the action of the second control loop in the TBA920.
For a line output stage with a BU108 high voltage transistor the resulting duration is about 22 μs, and in such a way that the line output transistor is switched on again about 8 μs after the middle of the line flyback pulse. This pulse duration must be taken into account when designing the driver stage and driver transformer as this way of driving the line output device differs from the usual, i.e. a driver duty cycle of about 50%.

CHARACTERISTICS (continued)

Oscillator

Frequency; free running (R_{15-16} = 3,3 kΩ)	f_o		15 625	Hz	1)
Spread of frequency at nominal values of peripheral components	$\frac{\Delta f_o}{f_o}$	<	±5	%	2)
Frequency change when decreasing the supply down to minimum 4 V	$\left\|\frac{\Delta f_o}{f_o}\right\|$	<	10	%	
Frequency control sensitivity	$\frac{\Delta f_o}{\Delta I_{15}}$	typ.	16,5	Hz/μA	
Adjustment range of network in circuit on page 6	$\frac{\Delta f_o}{f_o}$	typ.	±10	%	
Influence of supply voltage on frequency at V_P = 12 V	$\frac{\delta f_o}{f_o} \Big/ \frac{\delta V_P}{V_{Pnom}}$	<	5	%	

Control loop 1 (between sync pulse and oscillator)

Control voltage range	V_{12-16}		0,8 to 5,5	V	
Control current (peak values)					
at $V_{10-16} > 4,5$ V; $V_{6-16} > 1,5$ V	I_{12M}	typ.	±2	mA	
at $V_{10-16} < 2$ V; $V_{6-16} > 1,5$ V	I_{12M}	typ.	±6	mA	
Loopgain of APC system					
a. Time coincidence between sync pulse and flyback pulse or $V_{10-16} > 4,5$ V	$\frac{\Delta f}{\Delta t}$	typ.	1	kHz/μs	
b. No time coincidence or $V_{10-16} < 2$ V	$\frac{\Delta f}{\Delta t}$	typ.	3	kHz/μs	
Catching and holding range	Δf	typ.	±1	kHz	3)

1) The oscillator frequency can be changed for other t.v. standards by an appropriate value of C_{14-16}.

2) Exclusive external components tolerances.

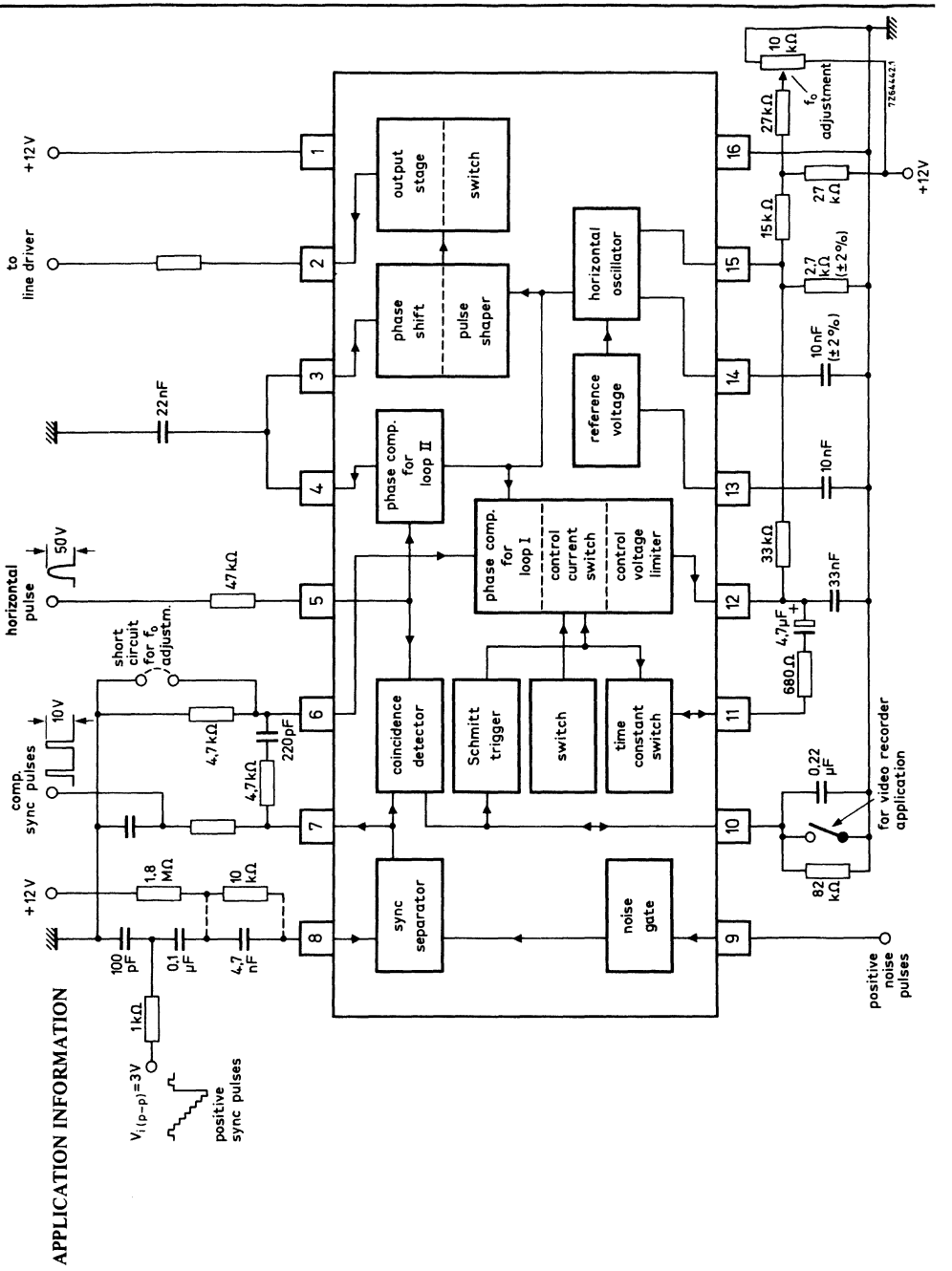
3) Adjustable with R_{12-15}.

CHARACTERISTICS (continued)

Pull-in time for $\Delta f/f_0 = \pm 3\%$ (Δf = 470 Hz)	t	≈	20	ms	1)
Switch-over from large control sensitivity to small control sensitivity after catching	t	≈	20	ms	1)
Control loop II (between flyback pulse and oscillator)					
Permissible delay between leading edge of output pulse (pin 2) and leading edge of flyback pulse	$t_{d\ tot}$		0 to 15	µs	
Static control error	$\frac{\Delta t}{\Delta t_d}$	<	0,5	%	2)
Output current during flyback pulse (peak value)	I_{4M}	typ.	±0,7	mA	
Overall phase relation					
Phase relation between leading edge of sync pulse and middle of flyback pulse	t	typ.	4,9	µs	3)
Tolerance of phase relation	$\lvert\Delta t\rvert$	<	1	µs	4)
Voltage for T_2 = 12 to 32 µs	V_{3-16}		6 to 8	V	
Adjustment sensitivity	$\frac{\Delta T2}{\Delta V_{3-16}}$	typ.	10	µs/V	
Input current	I_3	<	2	µA	
External switch-over of parameters (loop filter and loop gain) of control loop I (e.g. for video recorder application) see note 5.					
Required switch-over voltage					
at R_{11-16} = 150 Ω	V_{10-16}	>	4,5	V	
at R_{11-16} = 2 kΩ	V_{10-16}	<	2	V	
Required switch-over current					
at R_{11-16} = 150 Ω; V_{10-16} = 4,5 V	I_{10}	typ.	80	µA	5)
at R_{11-16} = 2 kΩ; V_{10-16} = 2 V	I_{10}	typ.	120	µA	

1) See application information circuit on page 6.
2) The control error is the remaining error in reference to the nominal phase position between leading edge of the sync pulse and the middle of the flyback pulse caused by a variation in delay of the line output stage.
3) This phase relation assumes a luminance delay line with a delay of 500 ns between the input of the sync separator and the drive to the picuture tube. If the sync separator is inserted after the luminance delay line or if there is no delay line at all (black-and-white sets), then the phase relation is achieved at C_{5-16} = 560 pF.
4) The adjustment of the overall phase relation and consequently the leading edge of the output pulse at pin 2 occurs automatically by the control loop II or by applying a d.c. voltage to pin 3.
5) With sync pulses at pin 7 and 8; without RC network at pin 10.

APPLICATION INFORMATION



COLOUR DEMODULATOR

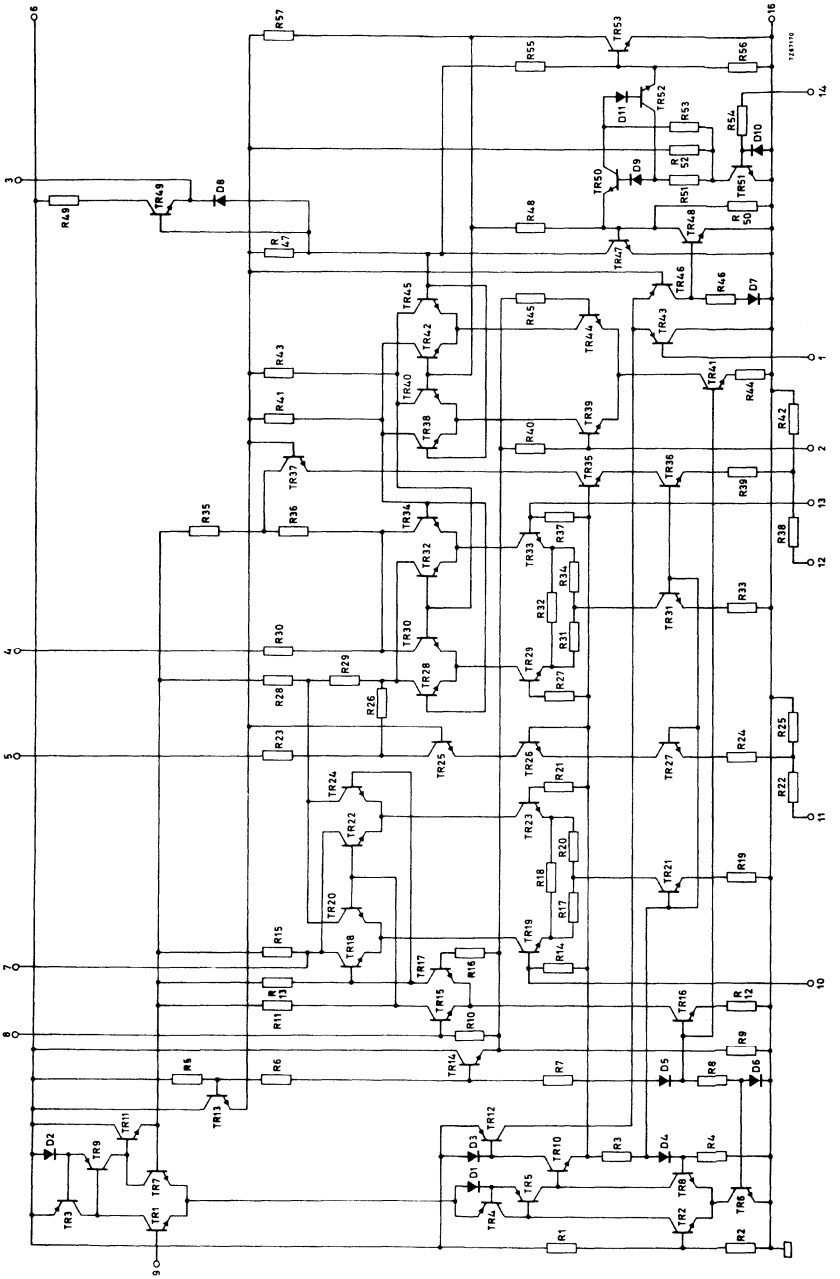
The TBA990 is an integrated colour demodulator circuit for colour television receivers incorporating two active synchronous demodulators for the R-Y and B-Y chrominance signals, a matrix (producing the G-Y colour difference signal), P.A.L. phase switch and flip-flop. It is suitable for d.c. -coupled drive to the picture tube when associated with the matrix integrated circuit (TBA530) and R.G.B. output stages.
Special attention has been given in the design to minimising d.c. level drift with temperature.

QUICK REFERENCE DATA			
Supply voltage (stabilised)	V_{6-16}	nom.	12 V
Supply current	I_6	nom.	17 mA
Gain of R-Y demodulator	G_{13-4}	typ.	3,8
Gain of B-Y demodulator	G_{10-7}	typ.	6,7
Impedance of chrominance inputs	$\left.\begin{matrix}\lvert Z_{13-16}\rvert \\ \lvert Z_{10-16}\rvert\end{matrix}\right\} >$		800 Ω in parallel with 10 pF
Impedance of colour-difference signal outputs	$\lvert Z_{4-16}\rvert$	typ.	3 kΩ
	$\lvert Z_{5-16}\rvert$	typ.	3 kΩ
	$\lvert Z_{7-16}\rvert$	typ.	3 kΩ

PACKAGE OUTLINES

TBA990 : 16 lead plastic dual in-line (type A) (See General Section)
TBA990Q: 16 lead plastic quadruple in-line (See General Section)

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_{6-16}	max.	13,2 V
Total power dissipation	P_{tot}	max.	300 mW
Temperatures			
Storage temperature	T_{stg}		−55 to +125 °C
Operating ambient temperature	T_{amb}		−20 to +60 °C

CHARACTERISTICS at V_{6-16} = 12 V (stabilised); T_{amb} = 25 °C

Gain of chrominance (R-Y) signal $V_{i(p-p)}$ = 50 mV; f = 4,4 MHz (see note 1)	G_{13-4}	typ.	3,8
Ratio of gain of blue channel to red channel defined at equal chroma signal inputs (see also pin 4 on page 6)	$\frac{G_{10-7}}{G_{13-4}}$	typ.	1,78
Matrix for generation G-Y signal			−0,51 (R-Y) −0,19 (B-Y)
Colour difference d.c. output voltage (see note 2)	V_{4-16}	typ.	7,5 V
	V_{7-16}	typ.	7,5 V
	V_{5-16}	typ.	7,5 V
Drift d.c. output voltage ΔT_{amb} = 40 °C; $V_{11-16} = V_{12-16}$ = 6 V		<	±50 mV
Relative change of d.c. output voltages between channels at ΔT_{amb} = 40 °C		<	20 mV
Colour difference output signals peak-to-peak values (see note 3): R-Y	$V_{4-16(p-p)}$	>	1,6 V
B-Y	$V_{7-16(p-p)}$	>	2,0 V
G-Y	$V_{5-16(p-p)}$	>	0,9 V
Impedance of chrominance inputs $V_{i(rms)}$ = 20 mV (sinusoidal); f = 4,4 MHz	$\lvert Z_{10-16}\rvert$ and $\lvert Z_{13-16}\rvert$	>	800 Ω in parallel with 10 pF
Impedance of reference signal inputs	$\lvert Z_{2-16}\rvert$	typ.	5 kΩ
	$\lvert Z_{8-16}\rvert$	typ.	5 kΩ
Impedance of colour-difference signal outputs	$\lvert Z_{4-16}\rvert$	typ.	3 kΩ
	$\lvert Z_{5-16}\rvert$	typ.	3 kΩ
	$\lvert Z_{7-16}\rvert$	typ.	3 kΩ

1. Ratio of peak-to-peak values of input and output signals.
2. These can be adjusted, by the potentiometers shown in circuit on page 5, by ±0,2 V to compensate for spreads in the matrix and output circuitry.
3. Linearity ≥ 0,7 measured in the circuit on page 5.

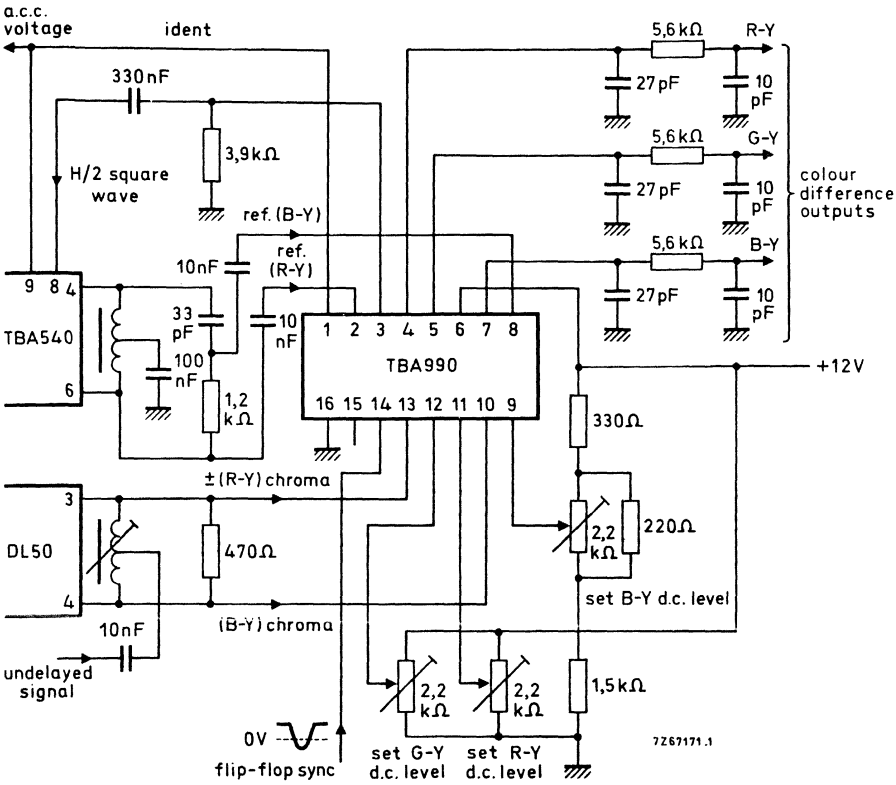
CHARACTERISTICS (continued)

Square wave output voltage			
peak-to-peak value; f = 7,8 kHz	$V_{3-16(p-p)}$	typ.	3,5 V
Input voltages			
Reference voltages (peak-to-peak)			
at reference R-Y	$V_{2-16(p-p)}$	typ.	1 V
at reference B-Y	$V_{8-16(p-p)}$	typ.	1 V
Identification circuit			
line pulse input (triggers on negative going edge)	$V_{14-16(p-p)}$		2 to 5 V
Identification signal			
required voltage for "ident on"	V_{1-16}	>	6,5 V
required voltage for "ident off"	V_{1-16}	<	5,5 V
required current for "ident on"	$-I_1$	<	0,1 mA
Input current			
Supply current consumption	I_6	typ.	17 mA

PINNING

1. Identification bias
2. R-Y sub-carrier reference input
3. P.A.L. square wave output (7,8 kHz)
4. R-Y signal output
5. G-Y signal output
6. Supply voltage (12 V)
7. B-Y signal output
8. B-Y sub-carrier reference input
9. B-Y d.c. level setting
10. B-Y chrominance input signal
11. G-Y d.c. level setting
12. R-Y d.c. level setting
13. R-Y chrominance input signal
14. Line pulse input (flip-flop synchronising)
15. n.c.
16. Earth (negative supply)

APPLICATION INFORMATION



APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number (see also page 5).

1. Identification bias

   The P. A. L. flip-flop is stopped, for identification purposes, when the voltage on pin 1 increases above 6 V. This threshold is internally generated and has a proportional behaviour with the 12 V supply voltage. The threshold level of 6 V is chosen to match the output characteristic of the TBA540 and has a sufficiently high safety margin above the zero chroma signal level of 4 V to eliminate spurious identifying.

2. R-Y subcarrier reference input

   A 1 V peak-to-peak signal is required via a d.c. blocking capacitor. Under no circumstances should this signal be less than 0,5 V peak-to-peak. The input resistance at this pin is typically 5 kΩ.

3. P. A. L. Square wave circuit

   The amplitude is 3,5 V peak-to-peak from an emitter follower.

4. R-Y signal output (G-Y at pin 5 and B-Y at pin 7)

   These outputs require no external d.c. loads except that direct connection must be made via the low pass filter to the appropriate pins on the R.G.B. matrix TBA530.

   The signals produced are in the following ratios:

   $$V_{B-Y} = 1,78\ V_{R-Y} \pm 10\ \%$$
   (a) $V_{G-Y} = 0,85\ V_{R-Y} \pm 10\ \%$
   (b) $V_{G-Y} = 0,17\ V_{R-Y} \pm 10\ \%$

   Condition (a) refers to (B-Y) + (R-Y) addition in the G-Y matrix.

   Condition (b) refers to the phase reversed (R-Y) input signal where (G-Y) is obtained by subtraction.

   The d.c. levels should each be adjusted, starting with the (B-Y), to +7,5 V at nominal supply voltage. However, in a complete circuit using the TBA530 matrix and feedback integrated circuit these d.c. levels will be adjusted to give the correct setting of the picture tube drive black levels.
   The changes in d.c. level with supply voltage are approximately linear and track together.

   The unwanted products of demodulation occurring in the colour difference outputs are chiefly 8,86 MHz and harmonics together with a small amount of 4,43 MHz due to possible unbalance in the demodulators. To avoid possible troubles in the receiver because of the radiation of these demodulation products from the R.G.B. drive circuits, filters must be employed in each of the colour-difference outputs from the TBA990. The roll-off should begin at about 1,5 MHz and attention should be given to the parallel resonance of the inductors to ensure that no serious attenuation will occur at less than 1,5 MHz. Also, some advantage may be secured by designing the inductor so that the dip due to its self-resonance occurs at about 4,43 MHz.

APPLICATION INFORMATION

5. G-Y signal output (see pin 4)

6. Positive supply

   The maximum allowable voltage on this pin is 13, 2 V.

7. B-Y signal output (see pin 4)

8. B-Y subcarrier reference input

   The requirements here are identical with those for pin 2.

9. D.C. level setting for B-Y output signal (see circuit diagram on page 5, and also pin 7)

10. Chrominance B-Y input signal

    An input signal of apprximately 360 mV peak-to-peak (colour bars) is required at this pin. The input impedance is greater than 800 Ω and the input capacitance is less than 10 pF. The spread in gain of the internal circuitry in the chrominance channel is ±10 %.

11. D.C. level setting for G-Y output signal (see circuit diagram on page 5, and also pin 5)

12. D.C. level setting for R-Y output signal (see circuit diagram on page 5, and also pin 4)

13. Chrominance R-Y input signal

    An input signal of approximately 500 mV peak-to-peak (colour bars) is required at this pin. The input impedance and spread in gain is the same as for pin 9.

14. Line pulse input (flip-flop synchronising)

    A waveform derived from the line timebase can be used for sychronising providing that its amplitude lies between 2 V and 5 V peak-to-peak. The trigger point occurs where the negative going edge crosses approximately +0, 6 V.

15. Not connected

    This pin should not be used for external connections.

16. Negative supply (earth)

INTEGRATED POWER AUDIO AMPLIFIER

The TCA160 is a monolithic integrated audio amplifier incorporating high flexibility for applications in battery and mains-fed equipment.
Due to special internal circuitry (stabilization, temperature correction, 20 dB feedback) the features are:
- negligible cross-over distortion over the entire supply voltage range (5 to 16 V).
- low quiescent current with low spread (5 to 15 mA) adjusted with a fixed resistor, so presetting is avoided.

Additional features are:
- high peak current (1 A).
- high unloaded supply voltage is tolerated (18 V).
- high gain (closed loop 50 dB at a feedback of 20 dB).
- safe operation regarding second breakdown.

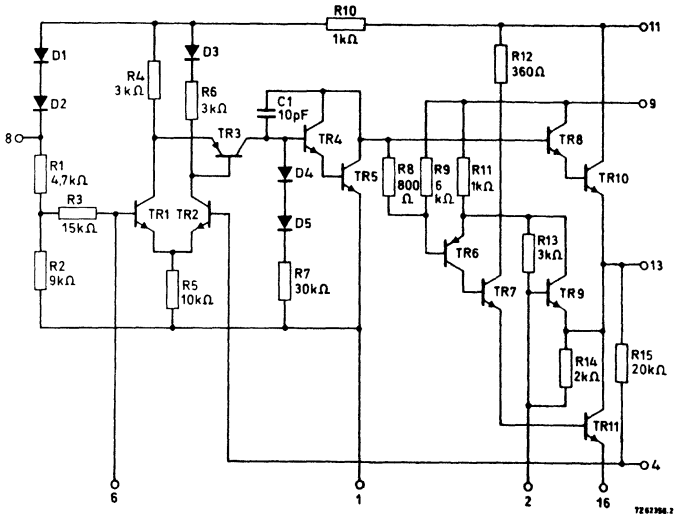
The special low thermal resistance envelope enables (at T_{amb} = 25 °C) a power dissipation of 0,9 W for TCA160 and 1,2 W for TCA160B without using an external heatsink.

QUICK REFERENCE DATA						
Supply voltage range			V_P		5 to 16	V
Total quiescent current			I_{tot}		5 to 15	mA
Unloaded supply voltage (peak value)			V_{PM}	max.	18	V
Output power			onset of clipping		d_{tot} = 10 %	
at V_P = 9 V; R_L = 8 Ω	P_o	typ.	0,9		1,0	W
Total distortion before clipping			d_{tot}	typ.	0,7	%
Input impedance			$\|Z_i\|$	typ.	15	kΩ
Sensitivity for d_{tot} = 10 %			V_i	typ.	10	mV

PACKAGE OUTLINE

TCA160 : 16 lead plastic power dual in-line (See page 9)
TCA160B : 16 lead plastic power dual in-line with cemented aluminium heat spreader (See page 10)

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Supply voltage (pin No. 11)	V_{11-16}	max.	16	V
Unloaded supply voltage (pin No. 11; peak value) (no signal condition)	V_{11-16M}	max.	18	V

Currents

Output current (pin No. 13, 11, 4)	I_O	max.	1	A
Non-repetitive peak output current (pin No. 13, 11, 4)	I_{OSM}	max.	2	A

Power dissipation [1])

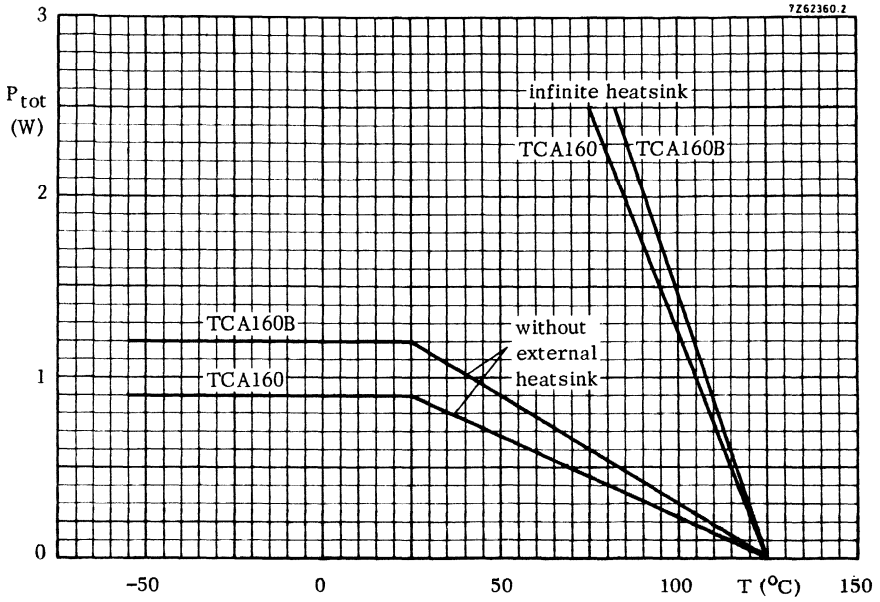
Dissipation without external heatsink at T_{amb} = 25 °C	TCA160 :	P_{tot}	max.	0,9	W
	TCA160B :	P_{tot}	max.	1,2	W

Temperatures

Storage temperature	T_{stg}	−55 to +125	°C
Operating ambient temperature	T_{amb}	−25 to +125	°C

1) See derating curve on page 3.

RATINGS (continued)



Design data

Pin No. 6 to No. 4 voltage	$\pm V_{6-4}$	max.	6	V
Pin No. 13 to No. 16 voltage	V_{13-16}	max.	16	V
Pin No. 11 to No. 13 voltage	V_{11-13}	max.	16	V

CHARACTERISTICS at T_{amb} = 25 °C; V_P = 9 V; R_L = 8 Ω unless otherwise specified

D.C. characteristics

Supply voltage range	V_{11-16}		5 to 16	V
Total quiescent current	I_{11tot}	typ.	8,7 5 to 15	mA mA 1)
Saturation voltages of output stages at I_o = 0.5 A	V_{CEsat}	<	0,9	V

A.C. characteristics

A.F. output power at onset of clipping	P_o	typ.	0,9	W
at d_{tot} = 10 %	P_o	typ.	1,0	W
Open loop voltage gain	G_v	typ.	70	dB
Total distortion before clipping	d_{tot}	typ.	0,7	%
Noise output power at R_S = 0	P_N	typ.	1,0	nW 1)2)
Signal to noise ratio at P_o = 1 W; R_S = 2 kΩ	S/N	typ.	80	dB 2)
Input sensitivity for d_{tot} = 10 %	V_i	typ.	10	mV
Input impedance	Z_i	typ.	15	kΩ

1) Measured with a.c. short circuited input.
2) Measured at a frequency ranging from 60 Hz to 15 kHz.

NOTES from page 5

1) Measured before output capacitor (C5),
2) Measured across R_L.
3) At R1 = 47 Ω. The gain can be increased by decreasing the value of R1; at decreasing the gain level however the maximum tolerated value of R1 amounts to 100 Ω; at further decrease of the gain an attenuator at the input is preferred.
4) To limit the frequency a capacitor must be connected across the input. For example: at R_S = 2 kΩ and C_x = 3,9 nF the upper frequency is 20 kHz (−3 dB). C_x also avoids oscillations at open input.
5) The lower limit can be decreased by a proportional increase of C3. e.g. at 60 Hz: C3 = 47 μF. Supply by-passing capacitor C2 also must be adapted to the lower frequency; at f_{min} = 60 Hz: C2 = 680 μF.
6) R_S = 0 Ω
7) R_S = 2 kΩ

APPLICATION INFORMATION (all values are typical)

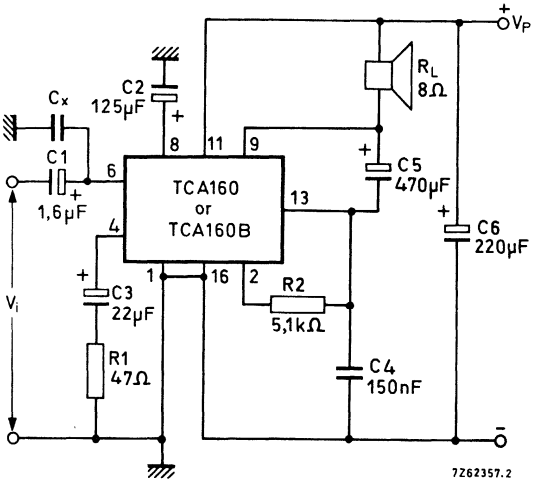
Supply voltage V_{11-16}	7,5	9	9	12	V	
Load resistance	4	4	8	8	Ω	
A.F. output power	0,9	1,2	1,0	1,5	W	1)
at onset of clipping	0,8	1,1	0,9	1,4	W	2)
A.F. output power	1,2	1,6	1,3	2,2	W	1)
at d_{tot} = 10 %	1,1	1,5	1,2	2,0	W	2)
Sensitivity						
for P_o = 50 mW V_i	1,4	1,4	2	1,8	mV	
for d_{tot} = 10 % V_i	7,3	8,0	10	13,0	mV	
Supply current for full output power	225	300	190	250	mA	
Quiescent current I_{tot}	8,1	8,7	8,7	8,6	mA	
Max. power dissipation	710	1020	510	910	mW	
Value of R1	47	47	47	47	Ω	
R2	5,1	5,1	5,1	5,1	Ω	
C1	1,6	1,6	1,6	1,6	μF	
C2	125	125	125	125	μF	
C3	22	22	22	22	μF	
C4	330	330	150	150	nF	
C5	1000	1000	470	470	μF	
C6	220	220	220	220	μF	
Input impedance Z_i	15	15	15	15	kΩ	
Closed loop voltage gain G_v	50	50	50	50	dB	3)
Open loop voltage gain G_v	70	70	70	70	dB	
Frequency responce	← 145 Hz to 110 kHz →					4)5)
Noise output power P_N	2,5	2,5	1,0	1,0	nW	6)
Noise output power P_N	19	19	9,5	10,2	nW	7)

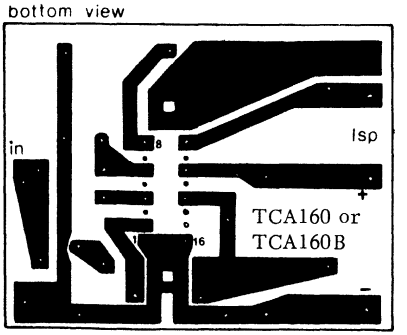
For notes see page 4

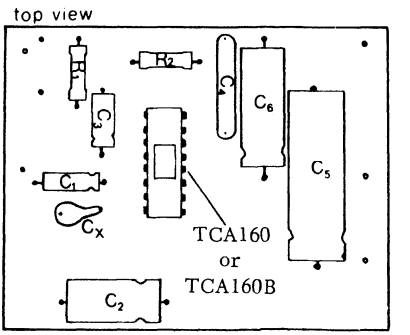
APPLICATION INFORMATION (continued)

General notes

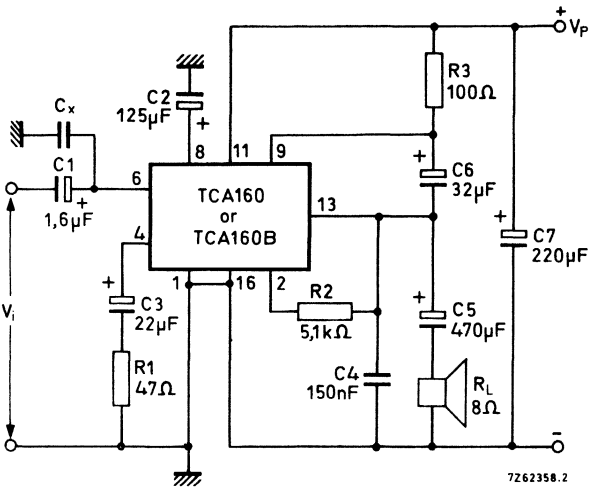
1. At using a mains-fed power supply with high ripple it is advantageous to connect the speaker to ground by bootstrapping pin 9 (see figure on page 7).
2. Prescription for print lay-out:
   Pin No. 1 must be used as a ground connection for the input circuit.
   Pin No. 16 must be used for the output circuit and for connection of the supply voltage.
   The pins No. 16 and 1 have to be interconnected as close to the package as possible to prevent a common impedance in the ground line.
3. The smoothing capacitor across the supply must be connected close to the pins.

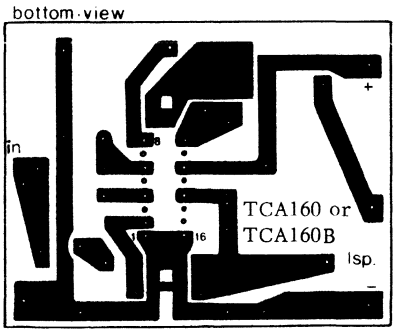


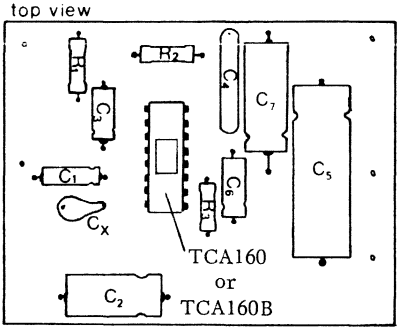


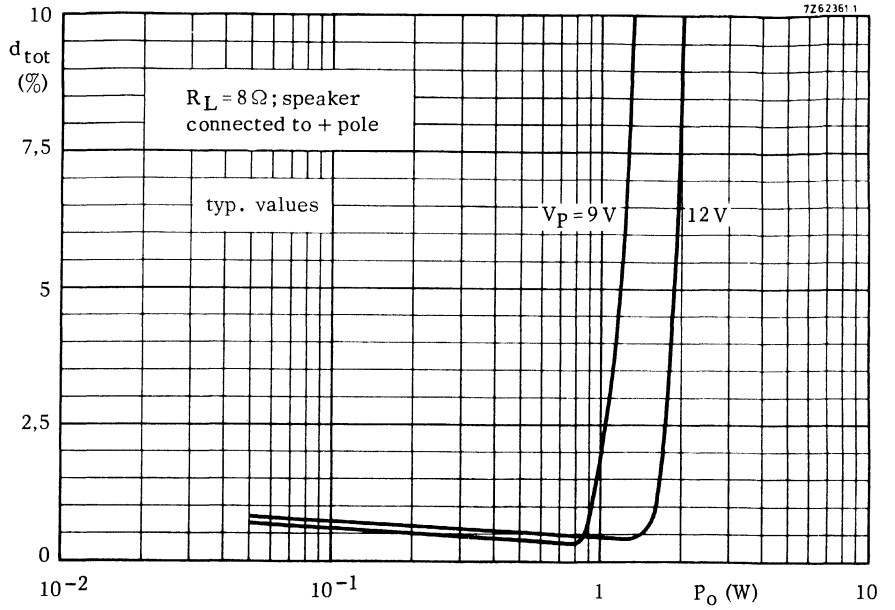


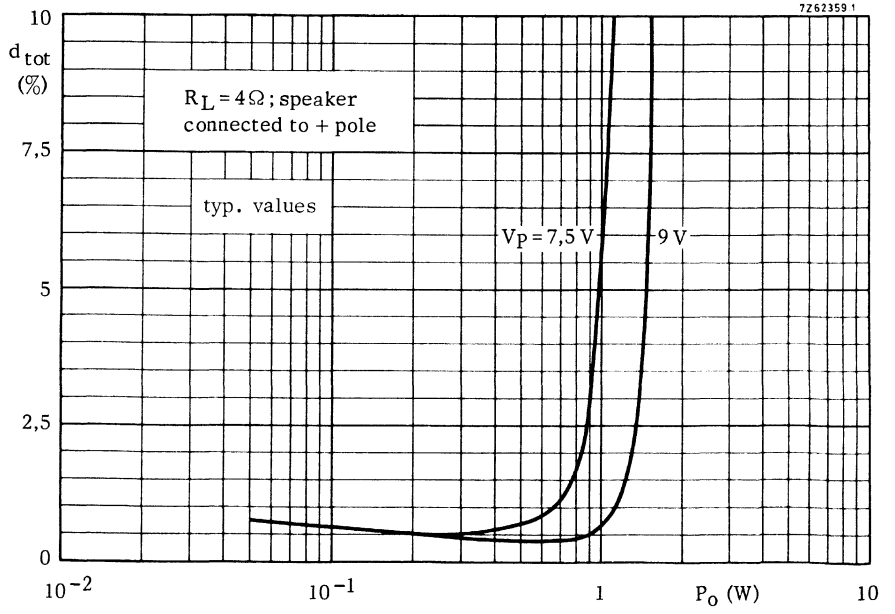
APPLICATION INFORMATION (continued)





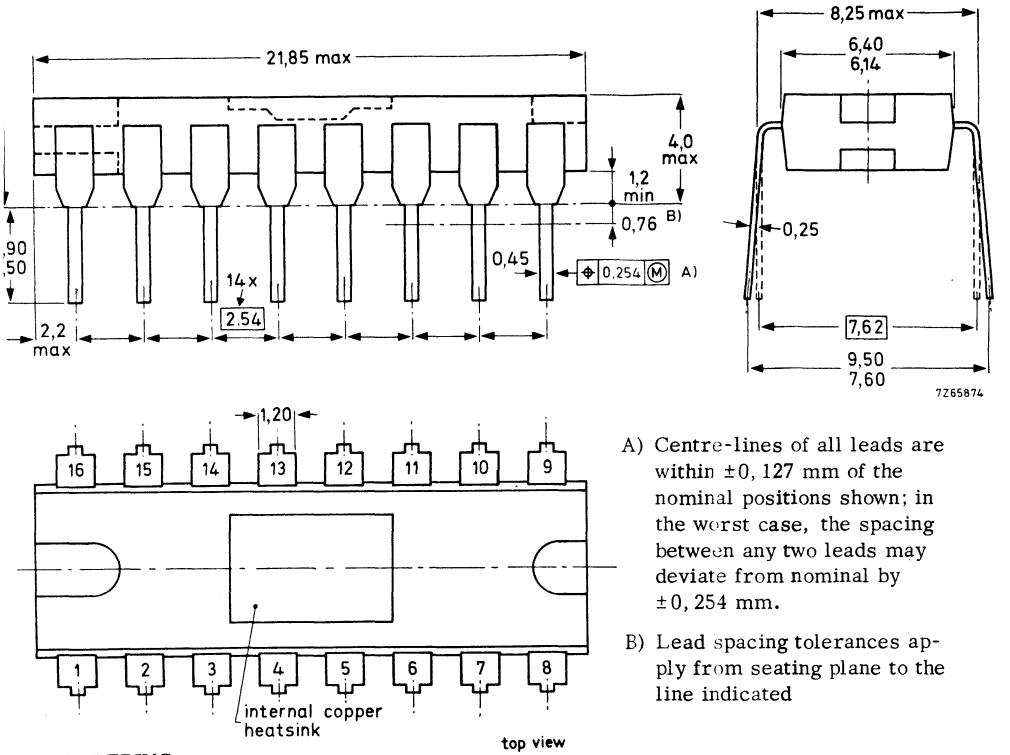



7Z62361.1
10
d_{tot} (%)
7,5
5
2,5
0
$R_L = 8\Omega$; speaker connected to + pole
typ. values
$V_P = 9$ V
12 V
10^{-2}
10^{-1}
1
P_o (W)
10


7Z62359.1
10
d_{tot} (%)
7,5
5
2,5
0
$R_L = 4\Omega$; speaker connected to + pole
typ. values
$V_P = 7{,}5$ V
9 V
10^{-2}
10^{-1}
1
P_o (W)
10

16 LEAD PLASTIC POWER DUAL IN-LINE

Dimensions in mm



A) Centre-lines of all leads are within ±0, 127 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0, 254 mm.

B) Lead spacing tolerances apply from seating plane to the line indicated

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

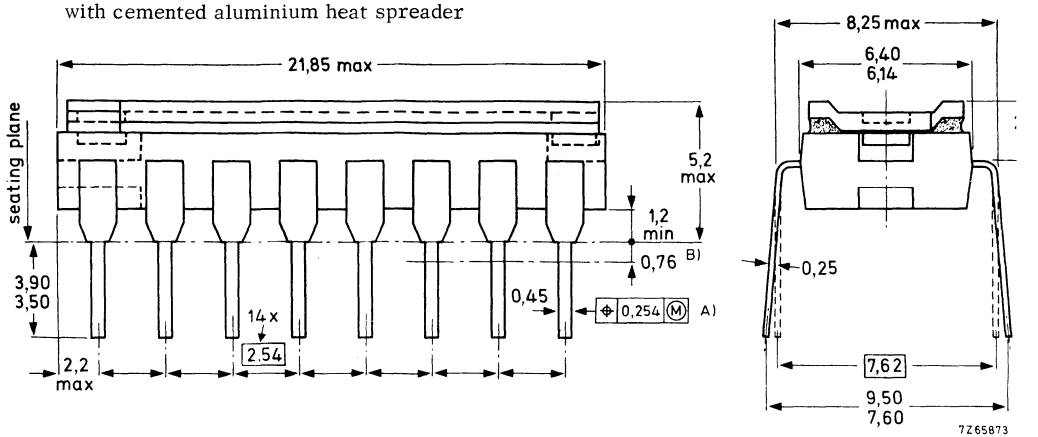
3. Repairing soldered joints

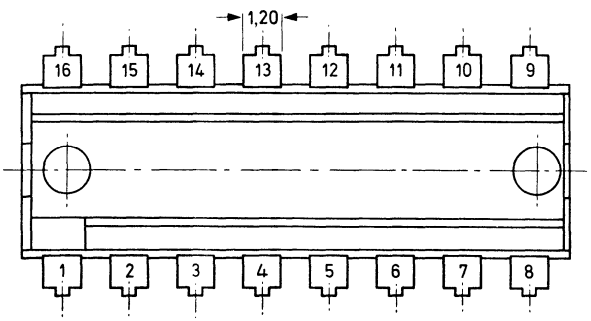
   The same precautions and limits apply as in (1) above.

16 LEAD PLASTIC POWER DUAL IN-LINE

with cemented aluminium heat spreader

Dimensions in mm





top view

A) Centre-lines of all leads are within ±0,127 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B) Lead spacing tolerances apply from seating plane to the line indicated

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

   The same precautions and limits apply as in (1) above.

AUDIO AMPLIFIER AND PRE-AMPLIFIER

The TCA210 is a monolithic integrated circuit comprising two amplifiers for use in intercoms and other audio systems. The first is a high-gain pre-amplifier with differential input and a class-A output stage which can deliver 2.5 mW into an 800 Ω load. The second is a power amplifier with a class-B output stage capable of delivering 500 mW into a 25 Ω load.

Speech rating: up to 800 mW can be delivered into a 15 Ω load for short periods.

When there is no signal, the current consumption is 8 mA (typ.). Squelch provision incorporated in both amplifiers can be used to ensure maximum battery life.

QUICK REFERENCE DATA				
Supply voltage	V_P	nom.	12	V
Total current drain	I_{tot}	typ.	8	mA
Pre-amplifier				
Open loop voltage gain	G_v	typ.	10 000	
Output power at R_L = 800 Ω	P_o	typ.	2.5	mW
Noise figure (B = 300 to 4000 Hz) R_S = 500 Ω	F	<	6	dB
Unity-gain bandwidth (compensated)	B	>	10	MHz
Output amplifier				
Open loop voltage gain	G_v	typ.	500	
Output power at R_L = 25 Ω; d_{tot} = 5 %	P_o	typ.	500	mW
at R_L = 15 Ω; d_{tot} = 5 %	P_o	typ.	800	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) (See General Section)

RATINGS (continued)

Temperatures			
Storage temperature	T_{stg}	−55 to +125	°C
→ Operating ambient temperature	T_{amb}	−55 to +125	°C 1)2)

CHARACTERISTICS at T_{amb} = 25 °C; V_P = 12 V

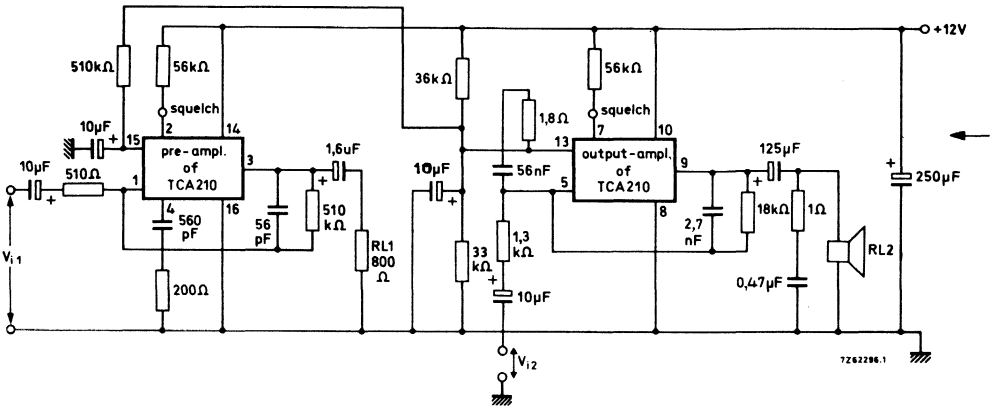
Pre-amplifier				
Open loop voltage gain	G_v	typ.	10 000	
Input bias current (pins 1 and 15)	$\frac{1}{2}(I_1+I_{15})$	typ.	2,5	µA
Unity gain bandwidth with 6 dB/oct compensation	B	>	10	MHz
→ Noise figure at R_S = 500 Ω; B = 300 to 4000 Hz	F	typ.	4	dB
Total current (pin 14)	I_{14}	typ.	4,0	mA
Current of current sink in output stage	I_C	>	2,5	mA
→ Bias current (pin 2)	I_2	>	200	µA
Output amplifier				
Open loop voltage gain	G_v	typ.	500	
Input bias current (pins 5 and 13)	$\frac{1}{2}(I_5+I_{13})$	typ.	2	µA
Unity gain bandwidth with 6 dB/oct compensation	B	>	1	MHz
Total current (d.c.; no signal; pin 10)	I_{10}	typ.	4	mA
Bias current (pin 7)	I_7	>	150	µA

1) See power derating curve on page 3.

2) To obtain good performance at low temperatures, high quality (tantalum) electrolytic capacitors must be used.

APPLICATION INFORMATION

Pre-amplifier and output amplifier for intercom systems



Performance T_{amb} = 25 °C; V_P = 12 V

Pre-amplifier

Output power at R_{L1} = 800 Ω	P_o	typ.	2,5	mW
Bandwidth (−3 dB)	B	typ.	4	kHz
Total current	I_{14}	typ.	4,0	mA
Input signal	V_{i1}	typ.	1,5	mV
Input impedance	$\|Z_i\|$	typ.	500	Ω

Output amplifier

Output power at R_{L2} = 25 Ω; d_{tot} = 5 %	P_o	typ.	500	mW
at R_{L2} = 15 Ω; d_{tot} = 5 %	P_o	typ.	800	mW ←
Bandwidth (−3 dB)	B	typ.	4	kHz
Total distortion at P_o = 50 mW	d_{tot}	typ.	1,5	%
Input signal	V_{i2}	typ.	260	mV
Input impedance	$\|Z_i\|$	typ.	1,3	kΩ ←
Total current (d.c.; no signal; pin 10)	I_{10}	typ.	4	mA

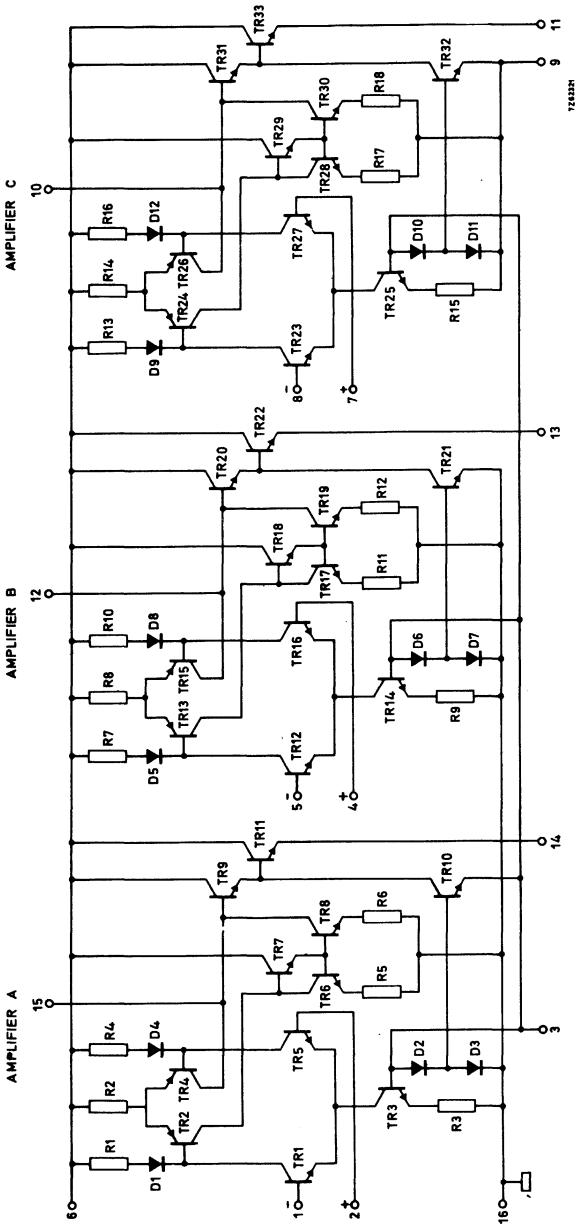
TRIPLE OPERATIONAL AMPLIFIER

The TCA220 is a monolithic integrated circuit, consisting of three identical high-gain amplifiers.
The amplifiers have a differential input stage and an emitter-follower output stage, which can supply a current up to 100 mA.
The unity-gain frequency with 6 dB/octave compensation is minimum 5 MHz. No latch-up occurs if the input voltage range is exceeded.

QUICK REFERENCE DATA				
Positive supply voltage	V_P	nom.	6	V
Negative supply voltage	V_N	nom.	6	V
Voltage gain	G_v	typ.	4000	
Common mode rejection ratio	CMRR	typ.	90	dB
Supply voltage rejection ratio	SVRR	typ.	200	μV/V
Input offset voltage	V_{io}	typ.	2	mV
Input offset current	I_{io}	typ.	0,2	μA

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

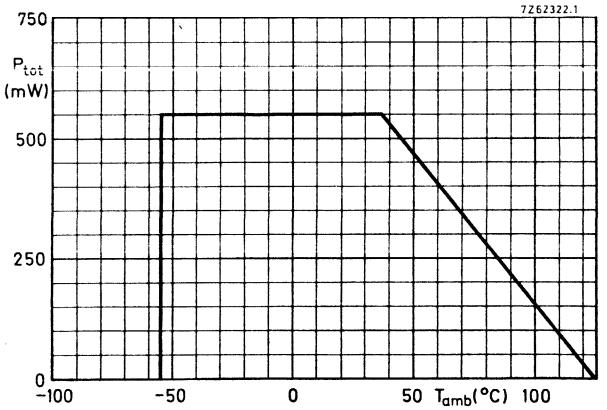
Voltages

Supply voltage	V_{6-16}	max.	18	V
Common mode input voltage	V_i	max.	18	V[1]
Differential input voltages	$\pm V_{1-2}$; $\pm V_{5-4}$; $\pm V_{8-7}$	max.	5,0	V
Pin No. 9 voltage	V_{9-16}	max.	0	V[2]

Currents

Input currents (pins, 1, 2, 4, 5, 7, 8)	I_1; I_2; I_4; I_5; I_7; I_8	max.	0,5	mA
Output currents (pins 14, 13, 11)	$-I_{14}$; $-I_{13}$; $-I_{11}$	max.	100	mA
Bias current (pin 3)	I_3	max.	5,0	mA

Total power dissipation



Temperatures

Storage temperature	T_{stg}	−55 to +125		°C
Junction temperature	T_j	max.	125	°C

1) For a total supply voltage less than 18 V, the absolute maximum input voltage is equal to the supply voltage.

2) If amplifier C is used, pin 9 must be connected to pin 16.

THERMAL RESISTANCE

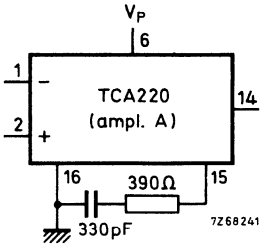
From junction to ambient	R_{th}	max.	160	°C/W

CHARACTERISTICS

(each amplifier) at V_P = 6 V; $-V_N$ = 6 V; T_{amb} = 25 °C
R_L = 10 kΩ (unless otherwise specified)

Voltage gain at ± V_{OM} = 3,5 V	G_v	typ.	4000	
Input offset voltage at $R_S \leq$ 200 Ω	V_{io}	typ.	2	mV
		<	10	mV
Input bias current	I_i	typ.	1,0	μA
		<	2,0	μA
Input offset current	I_{io}	typ.	0,2	μA
Common mode rejection ratio at R_S = 2 kΩ	CMRR	typ.	90	dB
Input voltage range	V_i	−4,3 to +5,6		V
Differential input resistance	R_i	>	25	kΩ
Supply voltage rejection ratio at R_S = 2 kΩ	SVRR	typ.	200	μV/V
Peak output voltage swing	V_{OM}	−6 to +3,5		V
Total current at V_o = 0; R_L = 10 kΩ	I_{tot}	typ.	1,0	mA
at V_o = 0; R_L = ∞	I_{tot}	typ.	0,4	mA
Slew rate (unity-gain)		typ.	0,4	V/μs
Bias current (all three amplifiers together)	I_3	>	200	μA [1]
Channel separation between amplifiers A and B		typ.	94	dB [2]
between amplifiers A and C		typ.	130	dB [2]
between amplifiers B and C		typ.	110	dB [2]

Frequency compensation circuit



1) The voltage at pin 3 is always 2 diode voltages (approx. 1,5 V) above the negative supply voltage; if the bias current in obtained from the positive supply voltage a dropping resistor $R_P \leq \frac{V_P - V_N - 1,5}{200 \cdot 10^{-6}}$
gives minimum power consumption.

2) Channel separation defined as 20 log $\frac{V_{oA}}{V_{oB}}$ x G_B, if G_B is the closed loop gain of amplifier B.

TELEVISION SIGNAL PROCESSING CIRCUIT

The TCA270 is a monolithic integrated circuit combining the following functions:
- synchronous demodulator
- video amplifier with buffer output stages
- noise inverters
- A.G.C. detector with output stages for n-p-n tuner and i.f. amplifier
- A.F.C. demodulator with buffer output stage

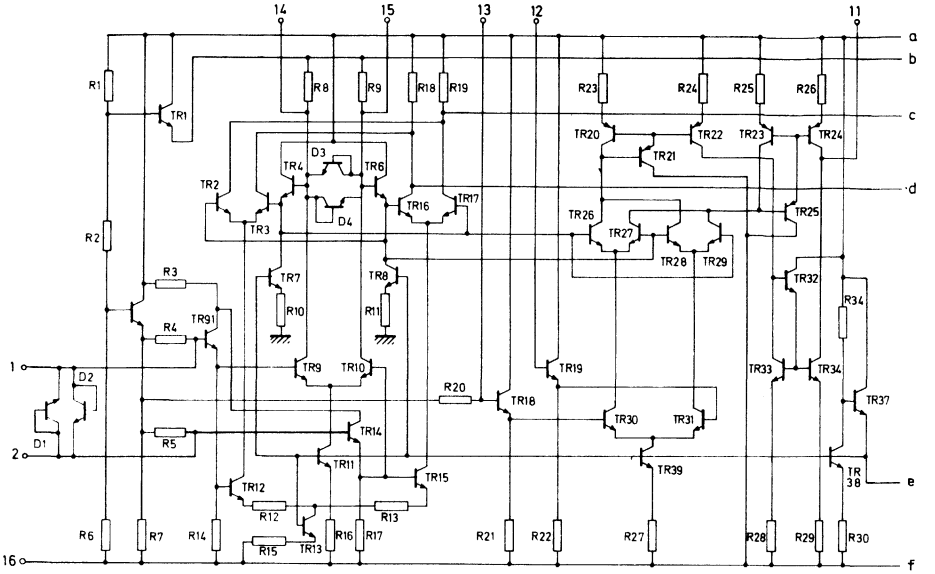
Opposite polarity video signals are available from emitter followers, the negative going signal being matched to integrated circuit type TBA920.

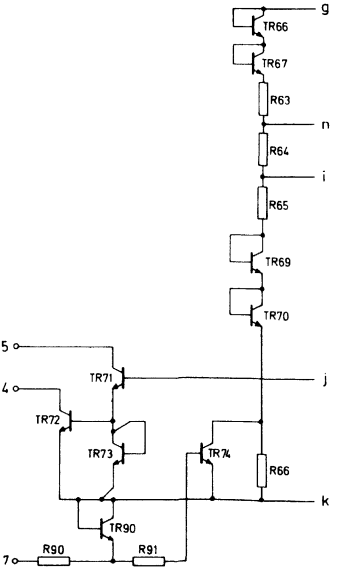
QUICK REFERENCE DATA				
Supply voltage	V_{3-16}	nom.	12	V
Ambient temperature	T_{amb}	typ.	25	°C
Frequency	f	typ.	38,9	MHz
Supply current	I_3	typ.	47	mA
Video output voltage (peak value)	V_{9-16M}	typ.	3	V
Bandwidth (3 dB)	B	typ.	5	MHz
Intermodulation products (blue colour bar)				
1,1 MHz w.r.t. B-W level		typ.	−60	dB
3,3 MHz w.r.t. B-W level		typ.	−67	dB
A.F.C. output control voltage swing (peak to peak value)	$V_{11-16(p-p)}$	>	10	V
A.G.C. control current for n-p-n i.f. (pin 4)	I_4	>	10	mA
A.G.C. control current for tuner (pin 5)	I_5	>	10	mA

PACKAGE OUTLINES

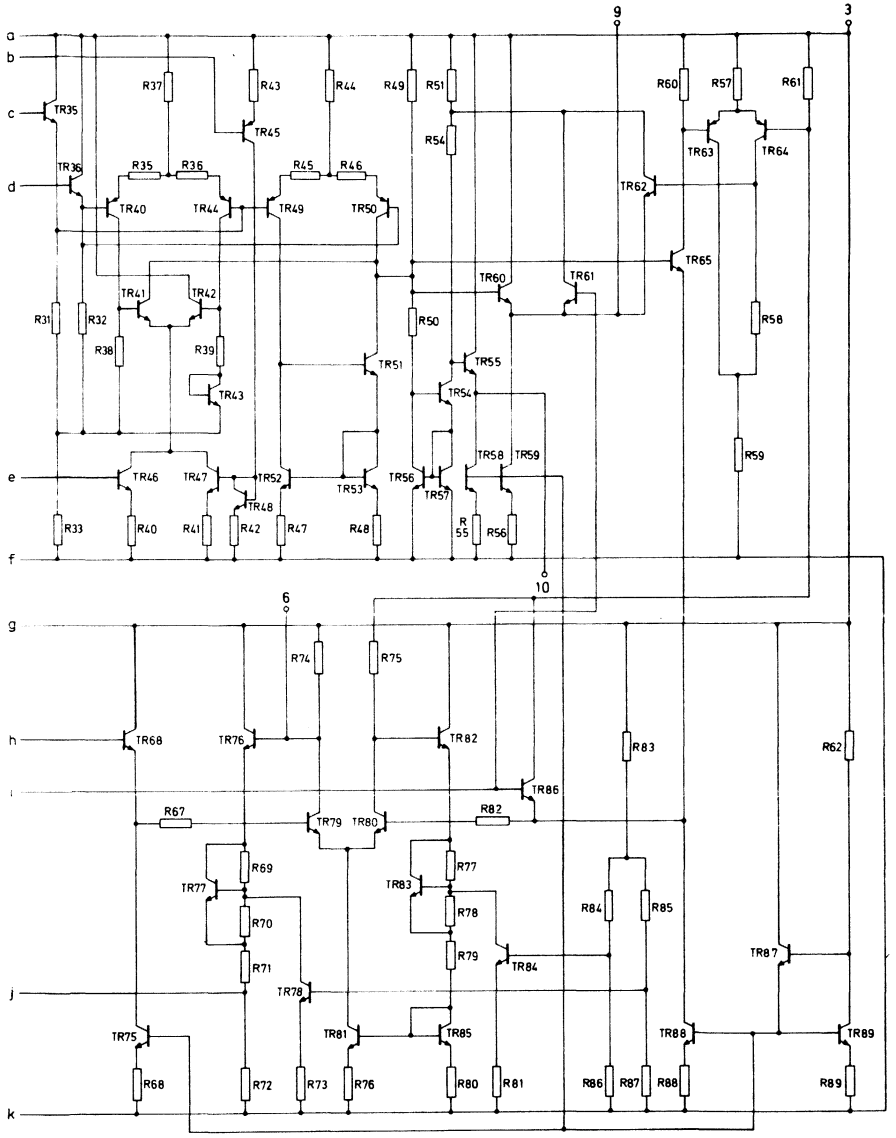
TCA270 : 16 lead plastic dual in-line (type A) (see general section)
TCA270Q : 16 lead plastic quadruple in-line (see general section)

CIRCUIT DIAGRAM





CIRCUIT DIAGRAM (continued)



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage during switch on ($t \leq 10$ s)	V_{3-16}	max.	18	V
Power dissipation	P_{tot}	max.	1	W
Temperatures				
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		−25 to +55	°C

CHARACTERISTICS

Supply voltage range	V_{3-16}	typ.	12,0	V
			10,2 to 13,8	V
Supply current range	I_3	typ.	47	mA
			33 to 62	mA
D.C. output voltage (zero signal; pin 9)	V_{9-16}	typ.	6	V
D.C. output voltage (zero signal; pin 10)	V_{10-16}	typ.	6	V
D.C. output voltage at start of a.g.c. (pin 9)	V_{9-16}	typ.	3	V
Unbalanced r.m.s. input voltage for a.g.c.	$V_{i(rms)}$	typ.	70	mV
			50 to 100	mV
Input resistance at pin 1	R_{1-16}	typ.	3	kΩ
Input resistance at pin 2	R_{2-16}	typ.	3	kΩ
Bandwidth (3 dB) of video output	B	typ.	5	MHz
Differential gain		<	10	% [1]
Differential phase		<	10	° [1]
Intermodulation products (blue colour bar)				
1,1 MHz		typ.	−60	dB
3,3 MHz		typ.	−67	dB
Carrier frequency rejection at pins 9, 10 and 11		>	40	dB
Twice carrier frequency rejection at pins 9, 10 and 11		>	40	dB

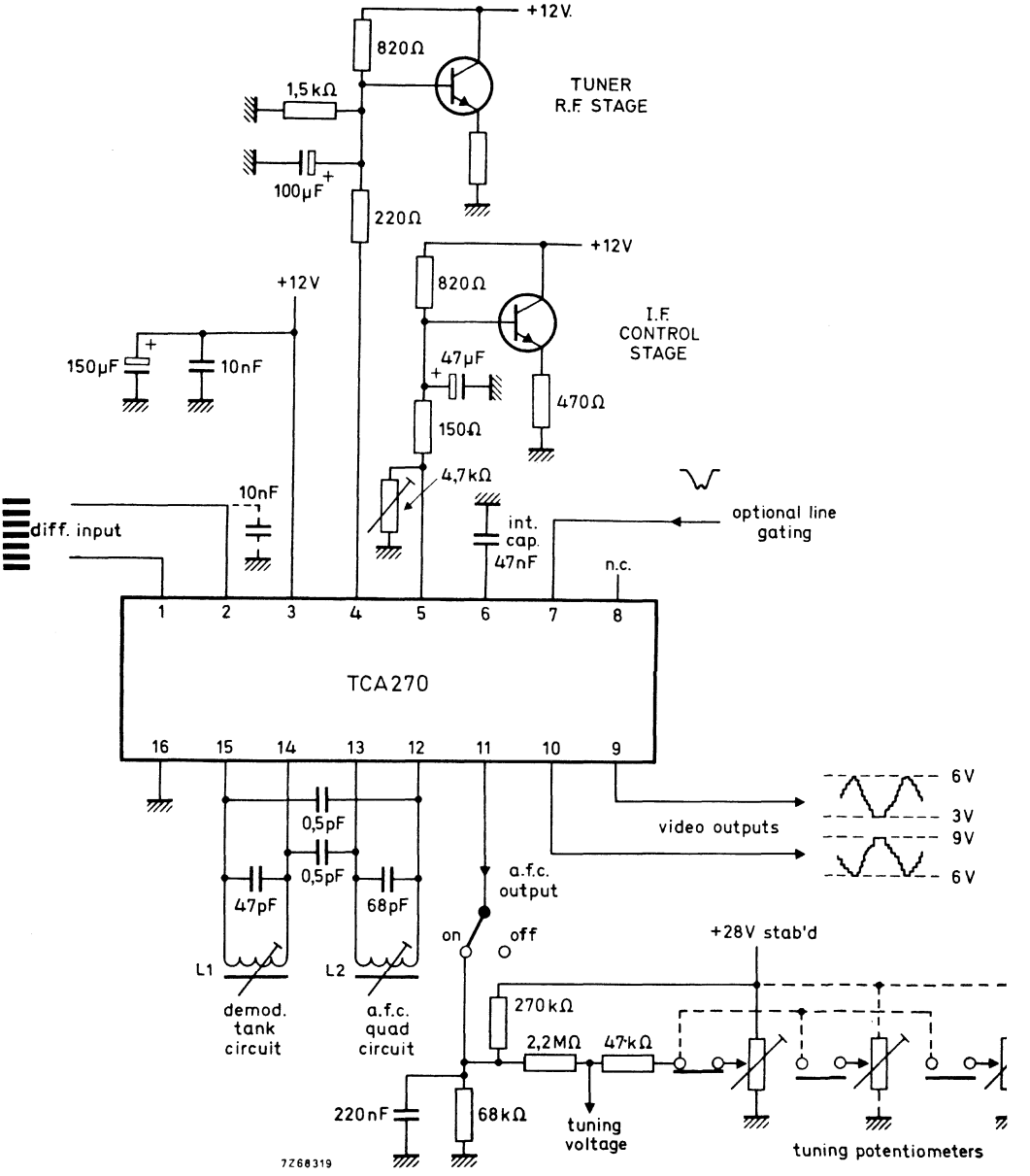
1) CCIR system of modulation, peak of white signal = 10% of carrier.

CHARACTERISTICS (continued)

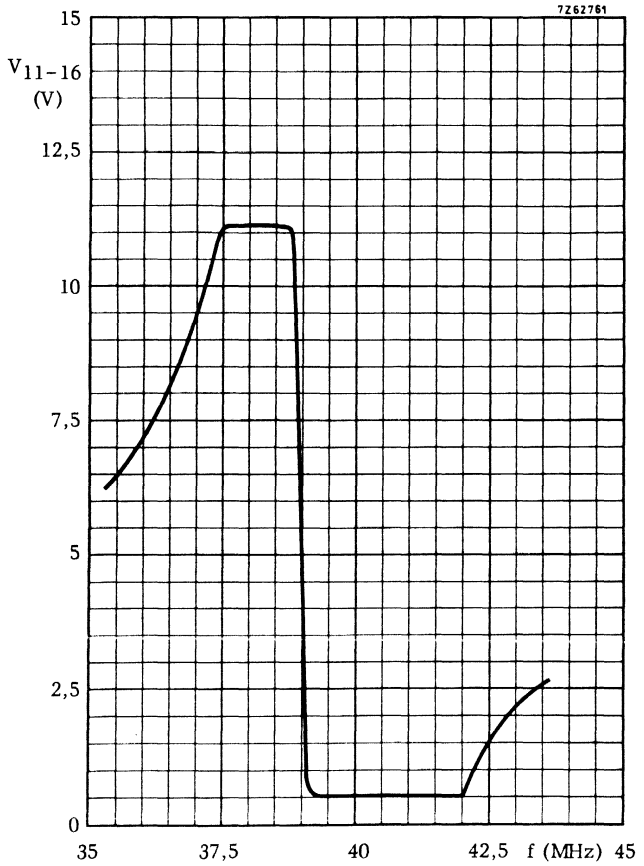
A.G.C. circuit				
Saturation voltage of tuner control at 10 mA (pin 4)	$V_{4\text{-}13sat}$	<	0,3	V
Saturation voltage of i.f. control at 10 mA (pin 5)	$V_{5\text{-}13sat}$	0,7 to	1,2	V
Breakdown voltage at 1 mA (pins 4 and 5)	$V_{(BR)4\text{-}13}$ $V_{(BR)5\text{-}13}$	>	14	V
Control current at pins 4 and 5	I_4; I_5	>	10	mA
Signal expansion for complete a.g.c.		<	0,5	dB
A.G.C. gating (optional) by negative line flyback pulse; input voltage (peak-to-peak value)	$V_{i(p\text{-}p)}$	> <	2 supply voltage	V
input resistance	R_i	typ.	1,8	kΩ
Current ratio of unsaturated outputs (pins 4 and 5) at I_5 = 1 mA	$\frac{I_4}{I_5}$	>	6	
A.F.C. circuit				
Output control voltage swing (peak-to-peak value)	$V_{11\text{-}16(p\text{-}p)}$	>	10	V
Change of frequency for complete output voltage swing		<	400	kHz
Change of frequency to maintain peak output voltage		>	±1	MHz
Noise inverters [1]				
Negative going noise pulses in pin 9 inversion threshold		typ.	2,55	V
Positive going noise pulses in pin 9 inversion threshold		typ.	6,6	V

1) Noise pulses are inverted to a point near black level.

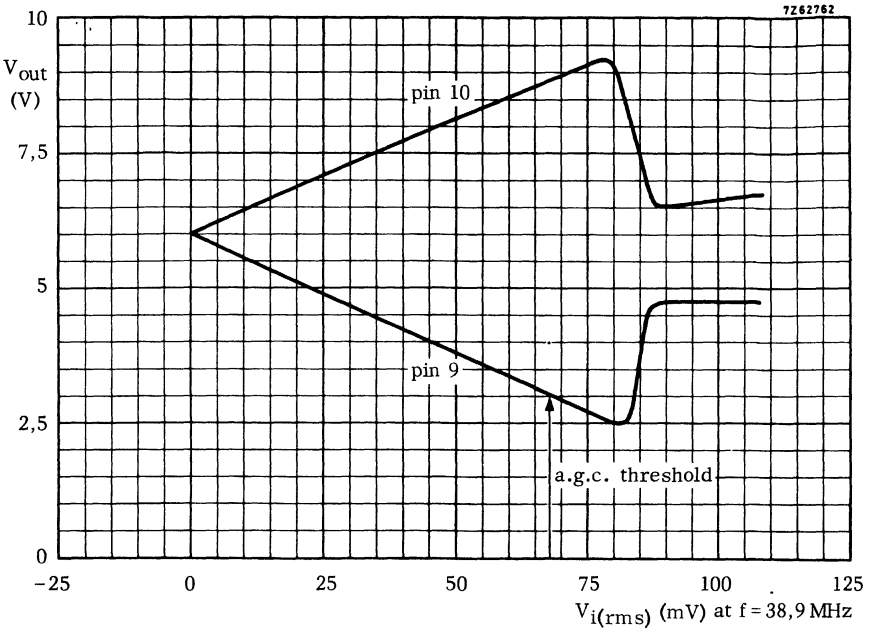
APPLICATION INFORMATION



Unloaded Q of L1 and L2 must be >50.



A.F.C. output voltage versus frequency



Transfer characteristic

F.M. STEREO DECODER

The TCA290A is a high quality monolithic integrated f.m. stereo decoder based on matrix decoding (frequency multiplexing).
The circuit provides automatic mono/stereo switching depending on both the pilot signal and the field strength and directly energizes a stereo indicator lamp. An external connection for mono/stereo switching is also available.

QUICK REFERENCE DATA			
Supply voltage (pin 7)	V_P	nom.	15 V
Ambient temperature	T_{amb}		25 °C
Distortion	d_{tot}	typ.	0,2 %
Cross-talk at f = 1 kHz	α	>	40 dB
19 kHz suppression	α_{19}	>	30 dB
		typ.	35 dB
38 kHz suppression	α_{38}	>	36 dB
		typ.	40 dB

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) (See General Section)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

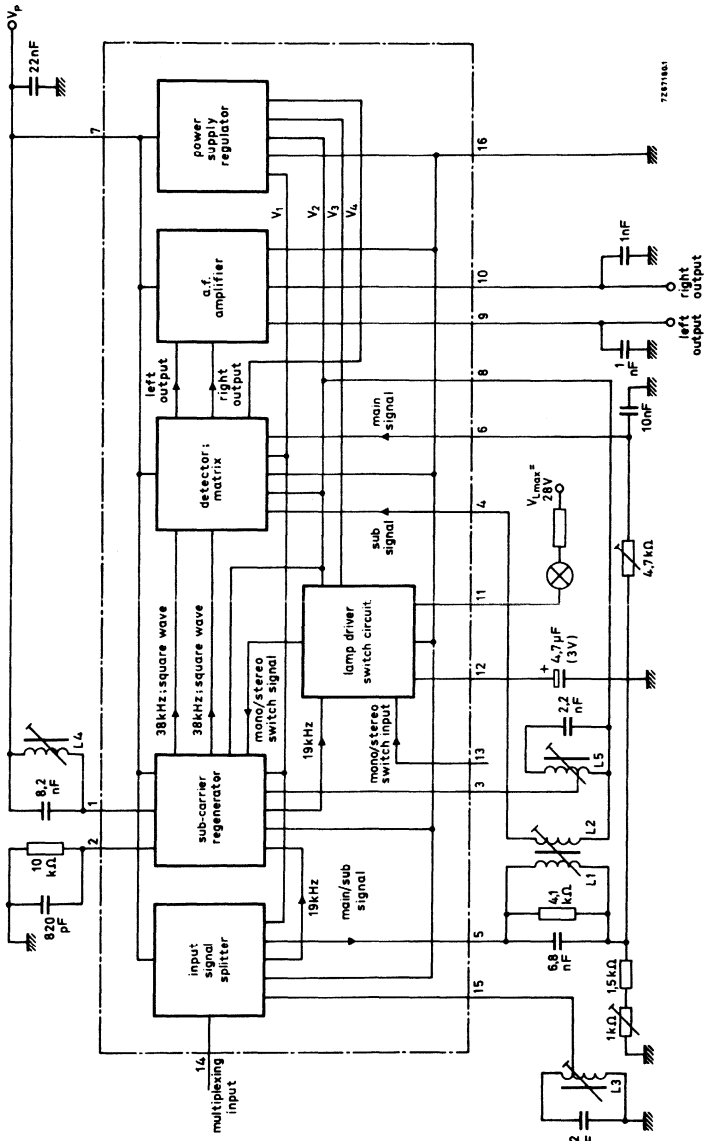
Voltages			
Supply voltage	V_{7-16}	max.	18 V
Indicator lamp voltage	V_{11-16}	max.	28 V[1])
Switching voltage mono/stereo	V_{13-16}	max.	3 V
Currents			
Indicator lamp current (d.c.)	I_{11}	max.	100 mA
Indicator lamp turn-on current (peak value)	I_{11M}	max.	200 mA
Dissipation			
Total power dissipation	P_{tot}	max.	500 mW
Temperatures			
Storage temperature	T_{stg}		−55 to +125 °C
Operating ambient temperature	T_{amb}		−30 to +80 °C

CHARACTERISTICS at T_{amb} = 25 °C; V_{7-16} = 15 V.

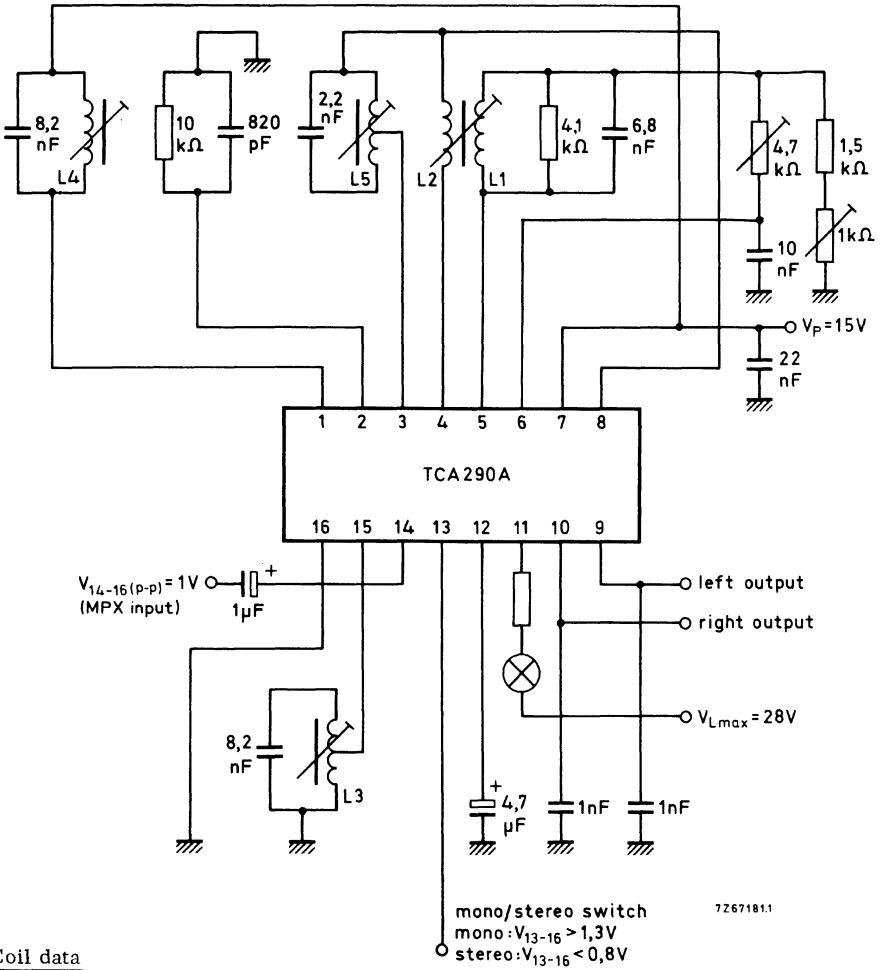
Input MPX voltage (peak-to-peak value)	$V_{14-16(p-p)}$	typ.	1 V
Input resistance (pin 14)	R_i	>	50 kΩ
Output resistance (pins 9 and 10)	R_o	typ.	5,6 kΩ
Distortion at f = 1 kHz; $V_{9-16(rms)}$ = 1 V; $V_{10-16(rms)}$ = 1 V	d_{tot}	typ.	0,2 %
Voltage gain defined as: $\frac{V_{9-16}}{V_{14-16}}$; $\frac{V_{10-16}}{V_{14-16}}$ at $V_{14-16(p-p)}$ = 1 V	G_v	typ. 2,5 to	3 4
Pilot-tone threshold switching voltage (r.m.s. value) at stereo "ON"	$V_{14-16(rms)}$	typ. 14 to 22	18 mV mV
Switching voltage			
to mono	V_{13-16}	>	1,3 V
to stereo	V_{13-16}	<	0,8 V
hysteresis		>	0,2 V
Total current (excluding indicator lamp)	I_{tot}	typ.	20 mA
Cross-talk at f = 1 kHz	α	>	40 dB
Ultra-sonic frequency rejection			
at 19 kHz	α_{19}	>	30 dB
		typ.	35 dB
at 38 kHz	α_{38}	>	36 dB
		typ.	40 dB
at 57 kHz	α_{57}	>	45 dB

[1]) Measured in test circuit on page 3.

CIRCUIT DIAGRAM



APPLICATION INFORMATION

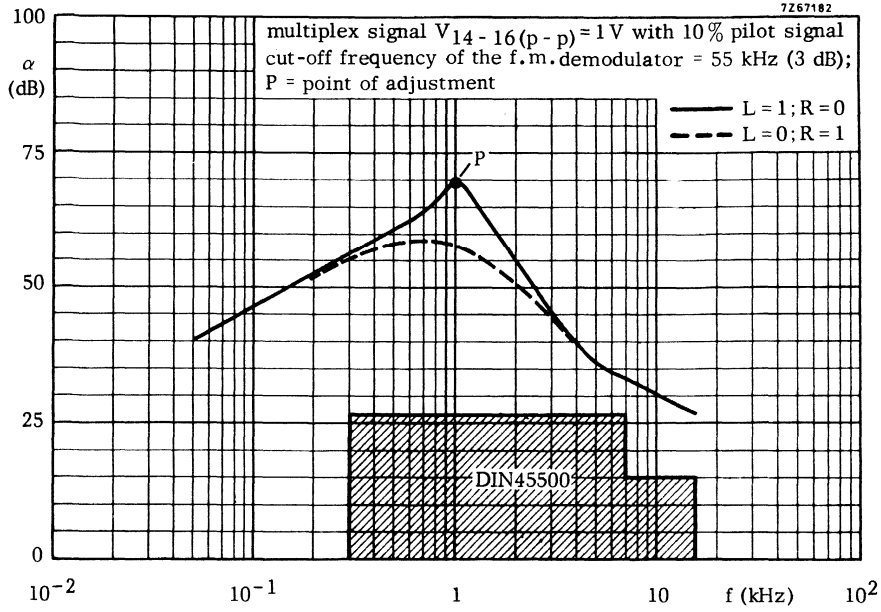


Coil data

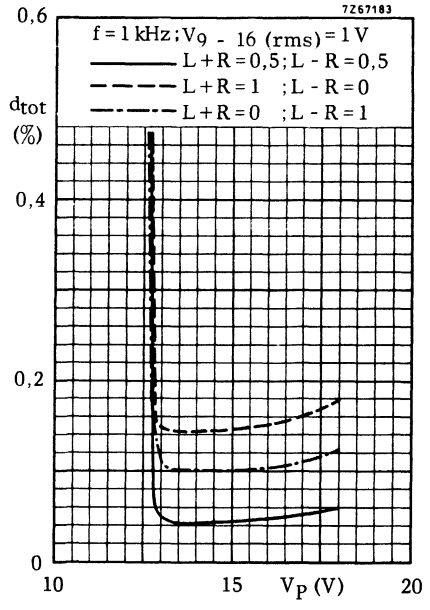
L1: 290 turns 0,1 mm e.c. wire
L2: 220 turns 0,1 mm e.c. wire (wound around L1) } Bandwidth: 6, 36 kHz
L3: 520 turns 0,1 mm e.c. wire (tapped at 130 turns from ground); $Q_o \approx 50$
L4: 520 turns 0,1 mm e.c. wire; $Q_o \approx 50$
L5: 520 turns 0,1 mm e.c. wire (tapped at 60 turns from pin 8); $Q_o \approx 80$

All coils wound on:

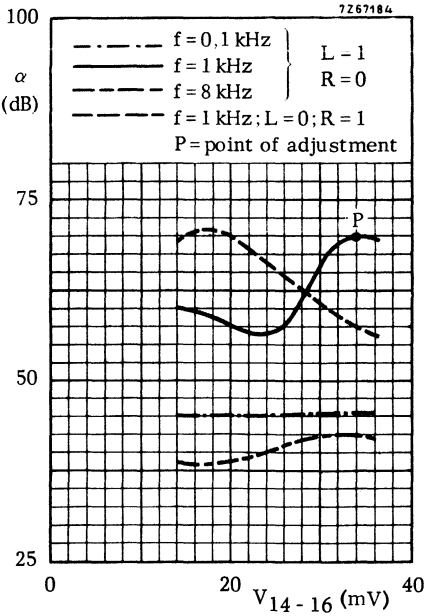
coil former : 4312 021 29650
window 3D3 : 4322 020 37030
screw core 3D3 : 4312 020 32150



Damping of cross-talk versus audio frequency.



Total harmonic distortion versus supply voltage.



Damping of cross-talk versus the 19 kHz input signal.

VOLTAGE FOLLOWER

The TCA410 is a silicon monolithic integrated operational amplifier internally connected as voltage follower.
Speacial futures are:

- very low input current
- continuous short citcuit protection
- no frequency compensation required
- small 4-lead package (TO-72)

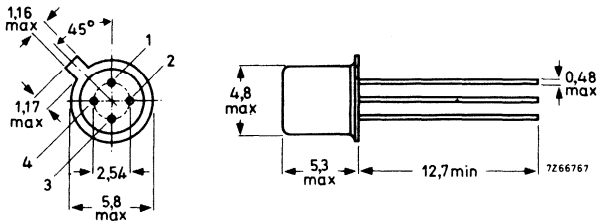
For most applications the TCA410 can be used as direct replacement of the LM302 and LM310.

QUICK REFERENCE DATA				
Supply voltage range	$V_P = V_N$		5 to 18	V
		TCA410A	TCA410B	
Input bias current	I_i	typ. 0,5	1,5	nA
Input offset voltage	V_{io}	typ.	3	mV
Peak output current	$\pm I_{OM}$	typ.	10	mA
Peak output voltage swing at R_L = 5 kΩ	$\pm V_{OM}$	typ.	13,5	V
Slew rate	S	typ.	4	V/μs

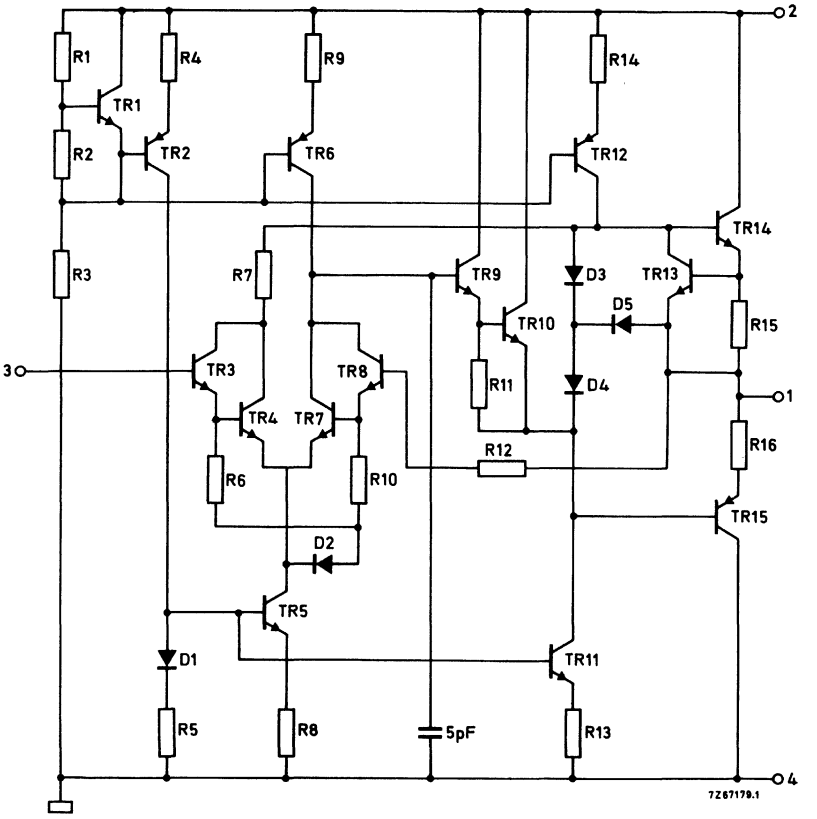
PACKAGE OUTLINE

Dimensions in mm

TO-72



CIRCUIT DIAGRAM



PINNING

1. Output
2. Positive supply (V_P)
3. Input
4. Negative supply (V_N) (connected to case).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

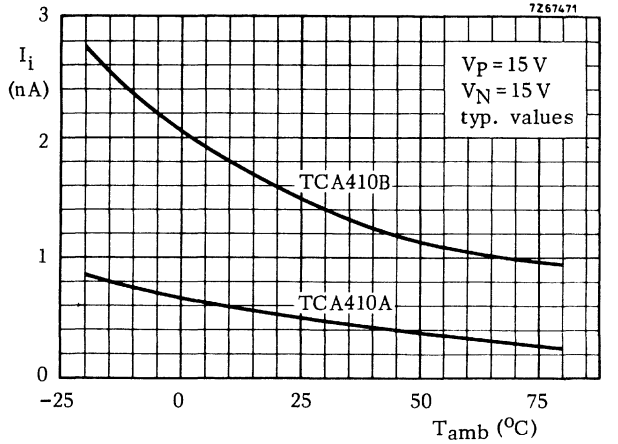
Voltages				
Positive supply voltage	V_P	max.	18	V
Negative supply voltage	V_N	max.	18	V
Input voltage	$\pm V_i$	max.	15	V [1]
Power dissipation (free air operation)	P_{tot}	max.	200	mW
Temperatures				
Operating ambient temperature	T_{amb}		−25 to +70	°C
Storage temperature	T_{stg}		−65 to +125	°C

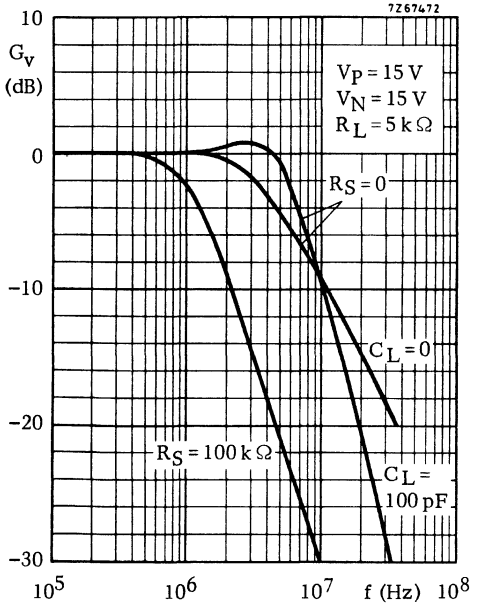
CHARACTERISTICS $V_P = 15$ V; $V_N = 15$ V; $T_{amb} = 25$ °C

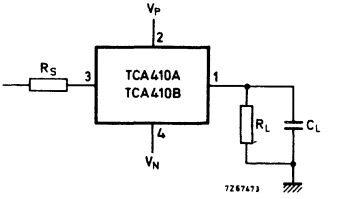
			TCA410A	TCA410B	
Input bias current	I_i	typ.	0,5	1,5	nA
		<	1,0	3,0	nA
Voltage gain at $R_L = 5$ kΩ	G_v	>		0,997	
		typ.		0,995	
Input offset voltage	V_{io}	typ.		3	mV
		<		10	mV
Peak output voltage swing at $R_L = 5$ kΩ	$\pm V_{OM}$	>		12,5	V [2]
		typ.		13,5	V [2]
Output short circuit current	$\pm I_o$	typ.		10	mA
				6 to 14	mA
Supply voltage range	$V_P = V_N$			5 to 18	V
Total supply current	I_{tot}	typ.		2,0	mA
		<		3,3	mA
Output impedance	$\lvert Z_o \rvert$	typ.		1	Ω
Total power dissipation at $V_o = 0$	P_{tot}	typ.		30	mW
		<		50	mW
Slew rate	S	typ.		4	V/μs

[1]) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to supply voltage.

[2]) The output voltage swing is always greater than: $V_P - 2,5$ V and $V_N + 2,5$ V.


7Z67471
3
2
1
0
I_i
(nA)
V_P = 15 V
V_N = 15 V
typ. values
TCA410B
TCA410A
−25
0
25
50
75
T_{amb} (°C)


7Z67472
10
G_v
(dB)
0
−10
−20
−30
V_P = 15 V
V_N = 15 V
R_L = 5 kΩ
R_S = 0
C_L = 0
R_S = 100 kΩ
C_L = 100 pF
10^5
10^6
10^7
f (Hz)
10^8


V_P
2
R_S
3
TCA410A
TCA410B
1
R_L
C_L
4
V_N
7Z67473

I.F. AMPLIFIER

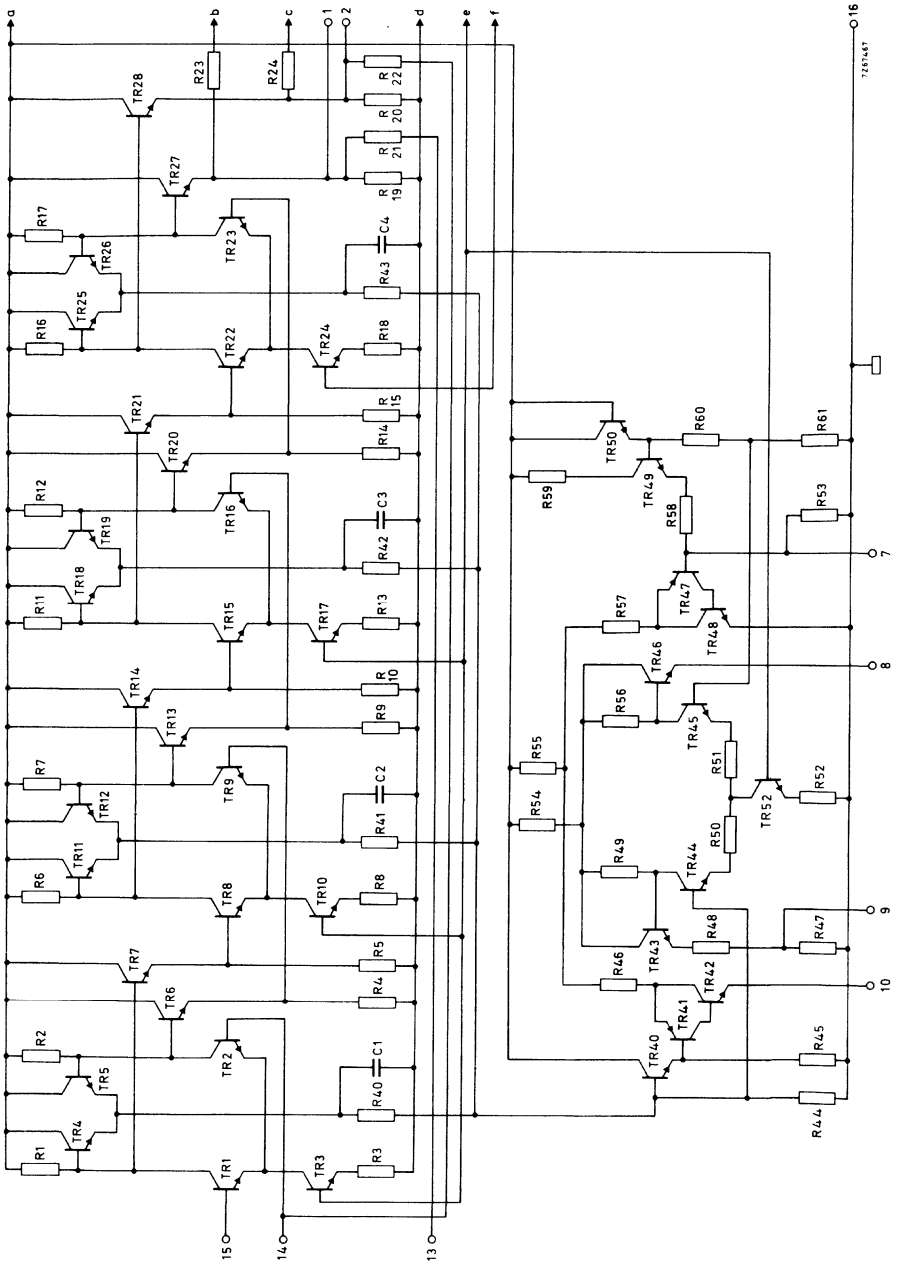
The TCA420A is a monolithic integrated i.f. amplifier for hi-fi f.m. receivers combining the following functions:

- f.m.-i.f. amplifier
- symmetrical f.m. detector
- a.f.c. voltage
- mono/stereo switching voltage
- field-strength depending indicator current
- automatic (adjustable) side response suppression

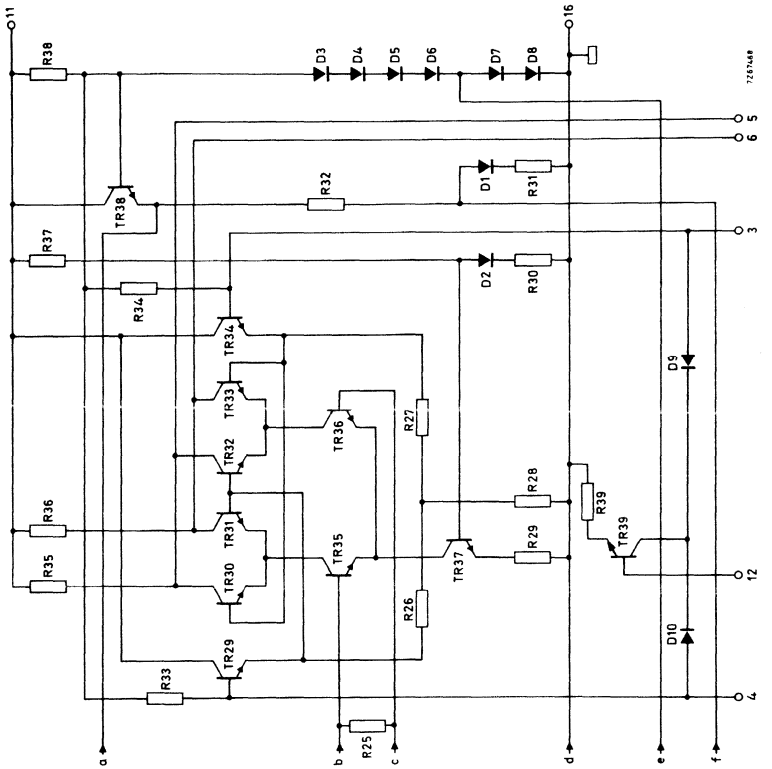
QUICK REFERENCE DATA				
Supply voltage	V_P	typ.	15	V
Ambient temperature	T_{amb}	typ.	25	°C
Frequency	f_o		10,7	MHz
Input limiting voltage (−3 dB)	V_{ilim}	typ.	35	μV
A.F. output voltage at $\Delta f = \pm 15$ kHz	V_{6-16}	typ.	115	mV
A.M. rejection at $\Delta f = \pm 15$ kHz; m = 0,3; f_m = 1 kHz; V_i = 10 mV	α	typ.	50	dB
Centre shift of f.m. detector curve at input voltage variation of 1 mV to 30 μV	$\lvert f_{o1}-f_{o2}\rvert$	typ.	7	kHz
I.F. voltage gain	G_v	typ.	65	dB

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



CIRCUIT DIAGRAM (continued)



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage				
Supply voltage (pin 11)	$V_P = V_{11-16}$	max.	18	V
Current				
Total current	I_{11}	max.	40	mA
Power dissipation				
Total power dissipation	P_{tot}	max.	720	mW
Temperatures				
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		−25 to +80	°C

CHARACTERISTICS at V_P = 15 V; T_{amb} = 25 °C; see circuit on page 7.

Output voltages (d.c. value) (pins 5 and 6)	V_{5-16}	typ.	9,5	V
	V_{6-16}		8,3 to 11	V
Voltage difference (d.c. value) (pins 5 and 6)				
at V_i = 1 mV	ΔV_{5-6}	<	350	mV
Current	I_{11}	typ.	26	mA
		<	35	mA
Input limiting voltage (−3 dB; R1 = 5 kΩ; pin 5)	$V_{i\,lim}$	typ.	35	μV
		<	50	μV

APPLICATION INFORMATION measured in the circuit on page 7 at following conditions:

f_o = 10,7 MHz; V_P = 15 V; T_{amb} = 25 °C; measured after adjustment to minimum distortion at: V_i = 1 mV, Δf = ±75 kHz, f_m = 1 kHz, R1 = 5 kΩ and C_{5-6} = 220 pF; a.c. values are measured on recommended printed circuit board on page 6.

A.F. output voltage				
Δf = ±15 kHz	V_{6-16}	>	95	mV
		typ.	115	mV
Total distortion at f_m = 1 kHz				
Δf = ±75 kHz	d_{tot}	typ.	0,8	%
		<	1,2	%
Δf = ±40 kHz	d_{tot}	typ.	0,3	%
Δf = ±15 kHz	d_{tot}	typ.	0,2	%

APPLICATION INFORMATION (continued)

A.M. rejection [1])

f.m. signal: $\Delta f = \pm 15$ kHz; $f_m = 70$ Hz
a.m. signal: m = 30%; $f_m = 1$ kHz; $V_i = V_{5-16}$

at $V_i = 0,3$ mV	α	>	40	dB
at $V_i = 1,0$ mV	α	>	40	dB
at $V_i = 10$ mV	α	>	45	dB
		typ.	50	dB
at $V_i = 100$ mV	α	>	40	dB

Signal to noise ratio

reference signal: $f_o = 10,7$ MHz; $\Delta f = \pm 15$ kHz; $f_m = 1$ kHz
noise signal : $f_o = 10,7$ MHz; without modulation
filter : $B_{(3\ dB)} = 250$ Hz to 16 kHz

at $V_i = 100$ mV	S/N	>	60	dB
at $V_i = 20\ \mu V$	S/N	typ.	26	dB

Centre shift of f.m. detector curve [2])

f.m. signal: $\Delta f = \pm 50$ kHz; $f_m = 70$ Hz
a.m. signal: m = 85%; $f_m = 1$ kHz

$\lvert f_{o1}-f_{o2} \rvert$	typ.	7	kHz
	<	15	kHz

I.F. voltage gain G_v typ. 65 dB

I.F. limited output voltages (peak-to-peak value)[3])

$V_i = 5$ mV; f = 1 MHz $V_{1-16(p-p)} = V_{2-16(p-p)}$

>	250	mV
typ.	350	mV

Input voltage levels for obtaining the required output voltages for switching a stereo decoder from mono to stereo vice-versa. These values are adjustable and the published levels are optimized for the TCA290A, where:
switching voltage to mono > 1,3 V
switching voltage to stereo < 0,8 V

Input voltage for $V_{10-16} = 0,8$ V

after adjusting R1, so $V_{R1} = 1,3$ V at $V_i = 0$ V_i

typ.	1,3	mV
	0,5 to 1,75	mV

Input voltage for $V_{10-16} = 1,3$ V

after adjusting R1, so $V_{R1} = 0,8$ V at $V_i = 3$ mV V_i

typ.	80	µV
<	200	µV

[1]) The interfering signal is measured with filter ($B_{(3\ dB)} = 700$ Hz to 5 kHz).

[2]) Defined as difference between frequency f_{o1} at $V_i = 1$ mV and frequency f_{o2} at $V_i = 30\ \mu V$. The frequencies f_{o1} and f_{o2} at equal voltages V_{5-6}.

[3]) Detector circuit not connected. Loads between pins 1-16 and 2-16 are equal: 10 MΩ in parallel with 8 pF.

APPLICATION INFORMATION (continued)

Field-strength indicator current

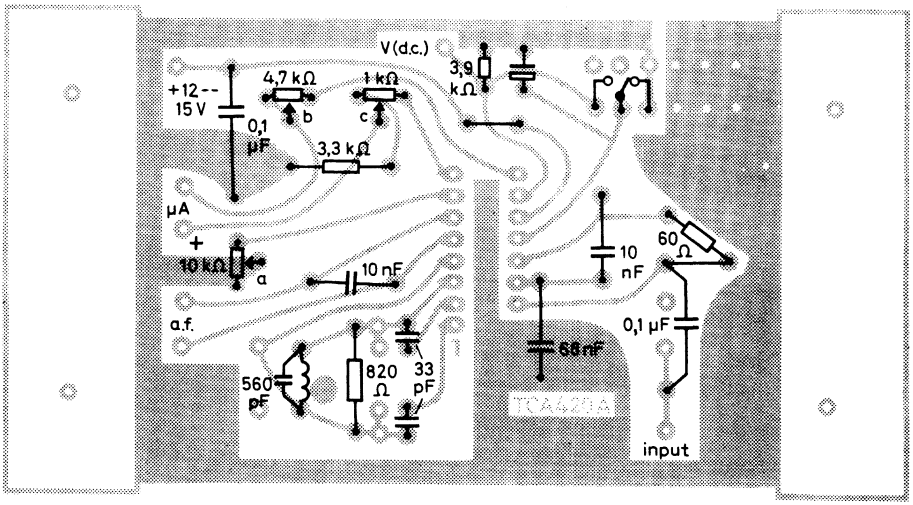
adjust R2 so $I_9 = 0$ at $V_i = 0$; R3 = 0; measured at V_i = 120 mV; $R_{indicator}$ = 2 kΩ	I_9	>	140	μA
		typ.	200	μA

Input voltage for 10 dB side response suppression

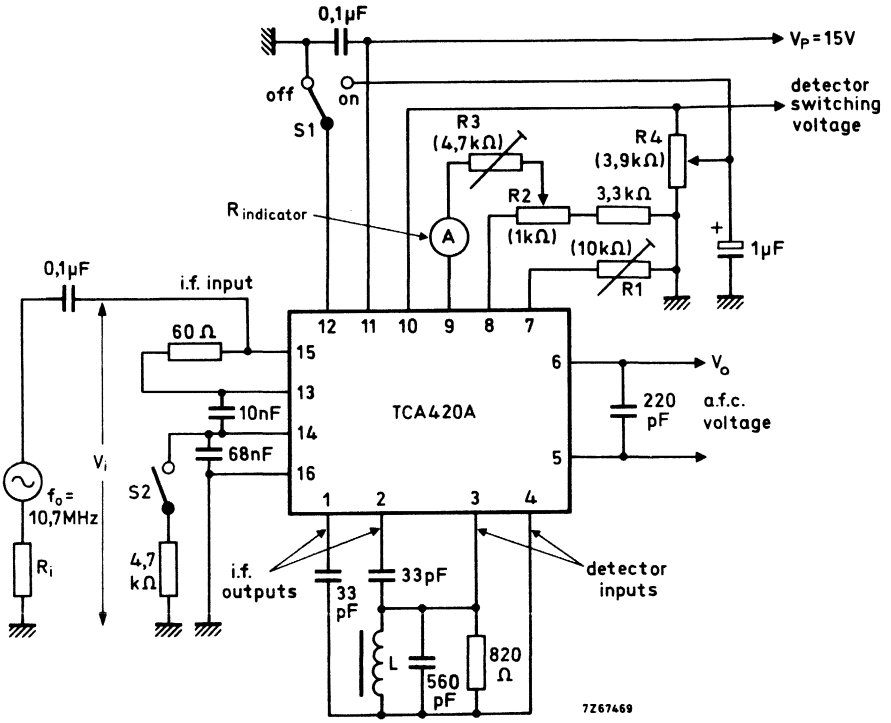
at S1 = "on" adjust R1, so V_{10-16} = 1,3 V at V_i = 0, S1 = "off"	V_i	typ.	40	μV

Output signal muting at S2 = "on"

reference signal at S2 = "off": V_i = 1 mV, f_m = 1 kHz, Δf = ±75 kHz	ΔV_o	>	60	dB



TEST CIRCUIT



Notes

V_{11-16} : supply voltage
V_{10-16} : switching voltage for stereo decoder (field strength dependent)
R1 : pre-set potentiometer for adjusting necessary output voltage V_{10-16}
R2 : pre-set potentiometer for adjusting the zero level of the field strength indicator current
R3 : pre-set potentiometer for adjusting the maximum level of the field strength indicator current
R4 : pre-set potentiometer for adjusting the side response suppression
S1 : side response suppression switch
S2 : output signal muting switch.

DUAL OPERATIONAL AMPLIFIER and STEREO PRE-AMPLIFIER

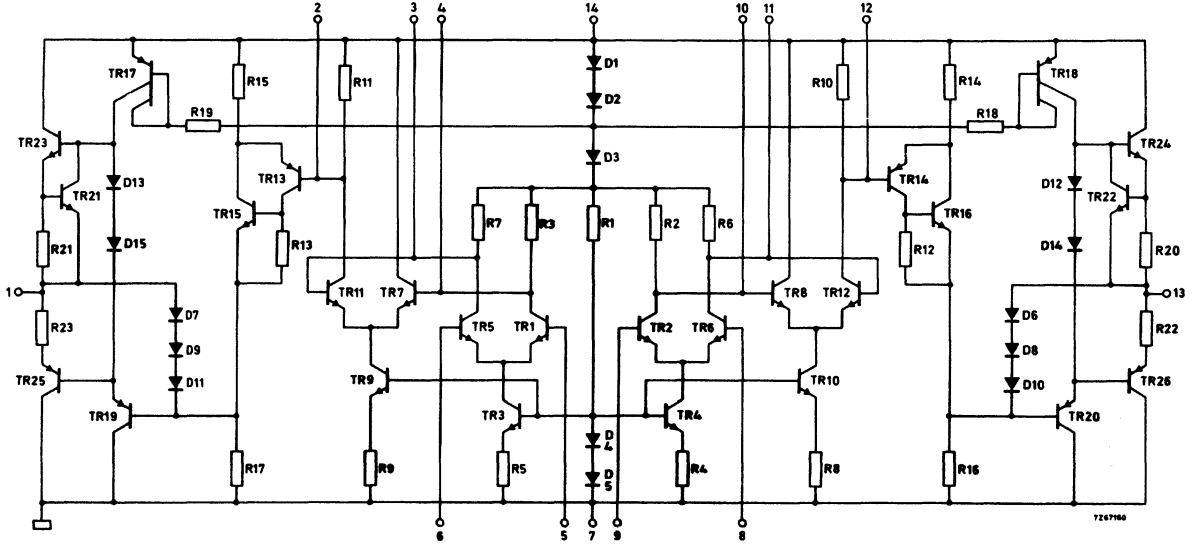
The TCA490A to C is a monolithic integrated circuit, consisting of two identical amplifiers. Primarily intended as a (stereo) audio amplifier it can also be used for general industrial purposes.
Special features are:

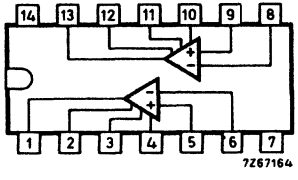
- **very low noise figure**
- **low distortion**
- **short circuit protection**
- **no latch up**
- **large output voltage swing**
- **usable as unity gain amplifier**

QUICK REFERENCE DATA						
Voltage gain	G_v		typ.	12 000		
Slew rate (gain = 10)			typ.	5		V/μs
		TCA490A	-B	-C		
Broadband noise figure	F	< 6	3	1,5		dB
Input noise voltage (r.m.s. value) (R.I.A.A.)	$V_{n(rms)}$	< 4	2,5	1,25		μV

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM





1. Output A
2. Lag output A
3. Lag input A
4. Lag input A
5. Non-inverting input A
6. Inverting input A
7. Negative supply (V_N)
8. Inverting input B
9. Non-inverting B
10. Lag input B
11. Lag input B
12. Lag output B
13. Output B
14. Positive supply (V_P)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages				
Positive supply voltage	V_P	max.	18	V
Negative supply voltage	V_N	max.	18	V
Differential input voltages	$\pm V_{5-6}$	max.	5	V
	$\pm V_{8-9}$	max.	5	V
Common mode input voltage	$\pm V_i$	max.	15	V [1]
Power dissipation	P_{tot}	max.	400	mW
Output short circuit duration	t	max.	30	s [2]
Temperatures				
Operating ambient temperature	T_{amb}		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

CHARACTERISTICS (each amplifier, see note 3) V_P = 12 V; V_N = 12 V; T_{amb} = 25 °C

Large signal voltage gain at $\pm V_o$ = 5 V	G_v	typ.	12 000	
			6 500 to 50 000	
Input offset voltage at $R_S \leq 200\ \Omega$	V_{io}	typ.	0,5	mV
		<	6,0	mV
Input bias current	I_i	typ.	250	nA
		<	1000	nA
Input offset current	I_{io}	typ.	30	nA
		<	500	nA
Common mode rejection ratio at $R_S \leq 10\ k\Omega$	CMRR	>	70	dB
		typ.	100	dB
Input voltage range	$\pm V_i$	typ.	9	V
Supply voltage rejection ratio at $R_S \leq 10\ k\Omega$	SVRR	typ.	50	μV/V
Peak output voltage swing at R_L = 2 kΩ	V_{OM}	>	8	V
Power dissipation (both amplifiers) at V_o = 0; I_o = 0	P_{tot}	typ.	160	mW

1) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

2) For one amplifier if short circuited to either supply or for both amplifiers if short circuited to ground.

3) If only one amplifier is used, either one of the input leads of the unused amplifier should be grounded.

CHARACTERISTICS (continued)

Slew rate at G_V = 10 compensation: R = 22 Ω; C = 10 pF			typ.	5	V/μs
Slew rate (unity gain) compensation: R = 0; C = 100 nF			typ.	0,5	V/μs
Broadband noise figure (see Fig. 1 below)		TCA490A	-B	-C	
R_S = 10 kΩ; B = 10 Hz to 10 kHz	F	< 6	3	1,5	dB
Input noise voltage (see Fig. 2 on page 5)					
(r.m.s. value) equalization R.I.A.A.	$V_{n(rms)}$	< 4	2,5	1,25	μV
Channel separation (see Fig. 3 on page 5) B = 100 Hz to 20 kHz			typ.	80	dB
Distortion at f = 1 kHz gain = 60 dB; $V_{o(rms)}$ = 5 V	d	<		1,5	%

TEST CIRCUITS

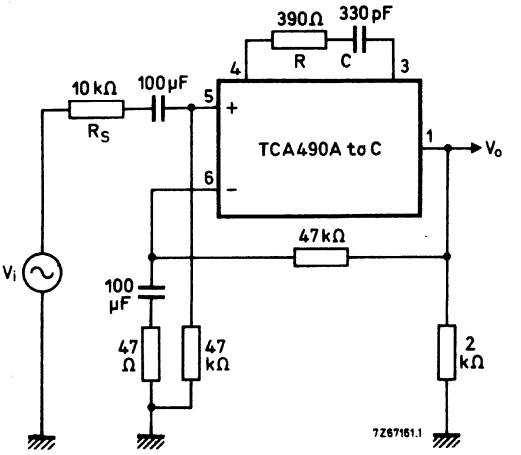


Fig. 1

TEST CIRCUITS (continued)

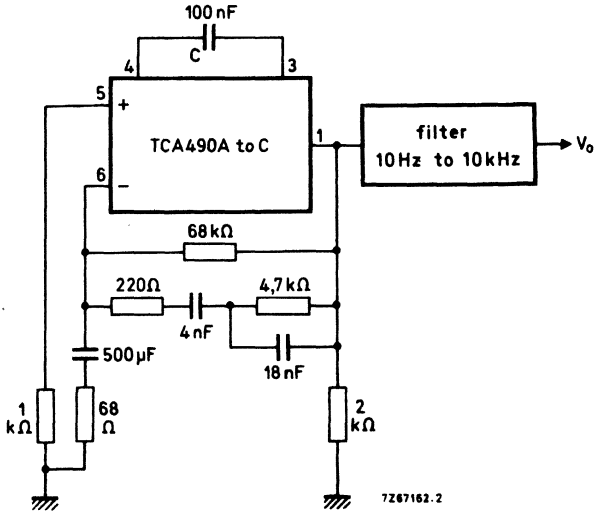


Fig. 2 Gain: 40 dB at 1 kHz. Input noise voltage = $\frac{V_n}{100}$

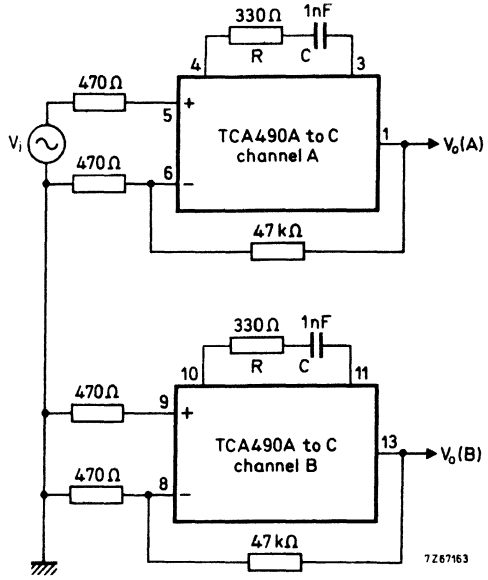
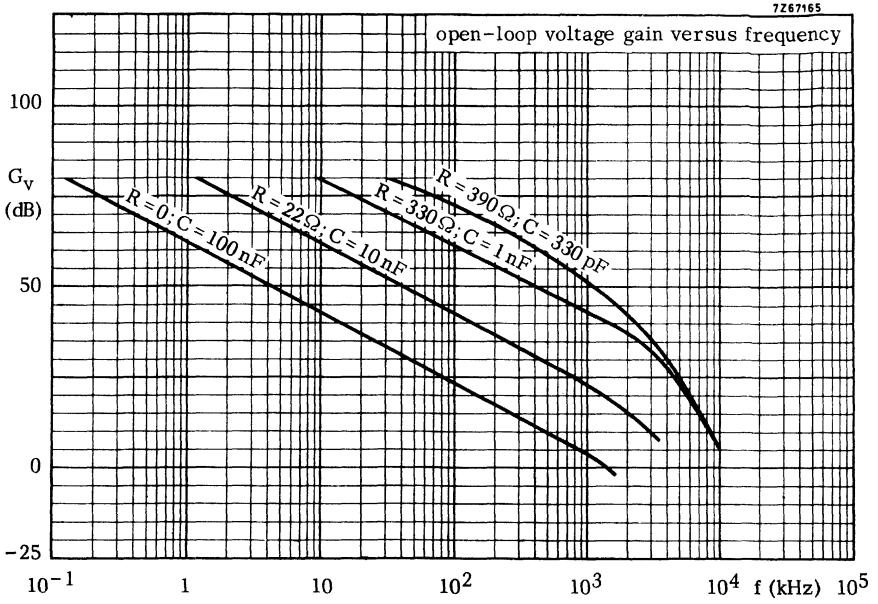
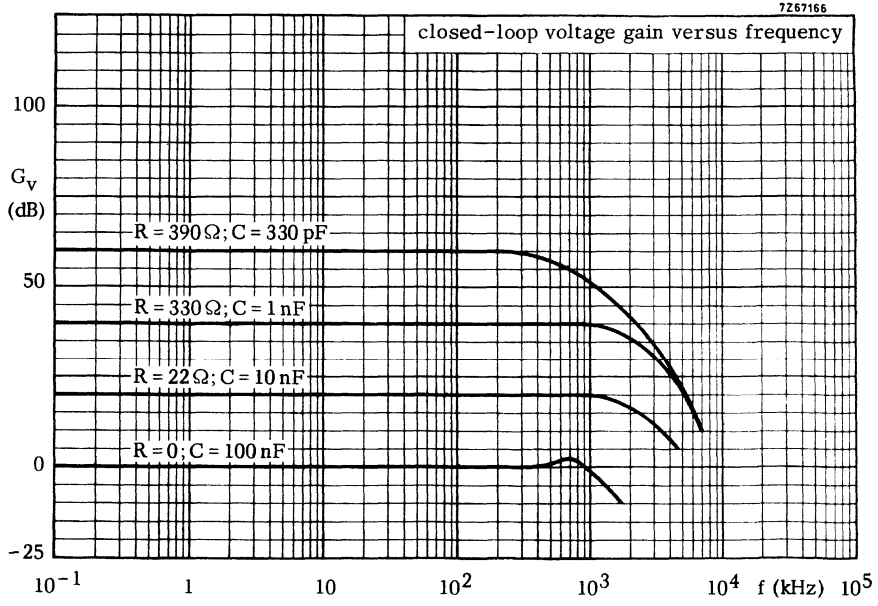


Fig. 3 Channel separation = $\frac{V_n\ (A)}{V_n\ (B)}$


7Z67165
open-loop voltage gain versus frequency
100
G_v
(dB)
50
0
−25
R = 0; C = 100 nF
R = 22 Ω; C = 10 nF
R = 330 Ω; C = 1 nF
R = 390 Ω; C = 330 pF
10^{-1}
1
10
10^2
10^3
10^4
f (kHz)
10^5


7Z67166
closed-loop voltage gain versus frequency
100
G_v
(dB)
50
0
−25
R = 390 Ω; C = 330 pF
R = 330 Ω; C = 1 nF
R = 22 Ω; C = 10 nF
R = 0; C = 100 nF
10^{-1}
1
10
10^2
10^3
10^4
f (kHz)
10^5

OPERATIONAL AMPLIFIER

The TCA520 is a silicon monolithic integrated circuit primarily intended for use in low power, low voltage applications and as comparator in digital systems.
Special features are:

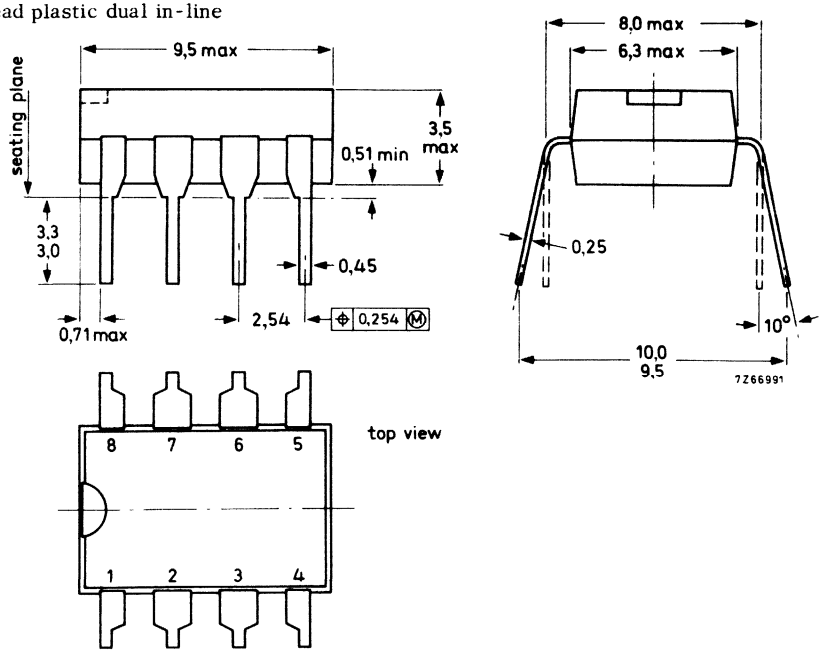
- large supply voltage range : 2 to 20 V
- offset voltage adjustable to zero
- output TTL -compatible
- low power consumption

QUICK REFERENCE DATA				
Supply voltage	V_P	nom.	5	V
Output sink current	I_{sink}	typ.	12	mA
Input current	I_i	typ.	30	nA
Slew rate (comparator)	S	typ.	50	V/μs

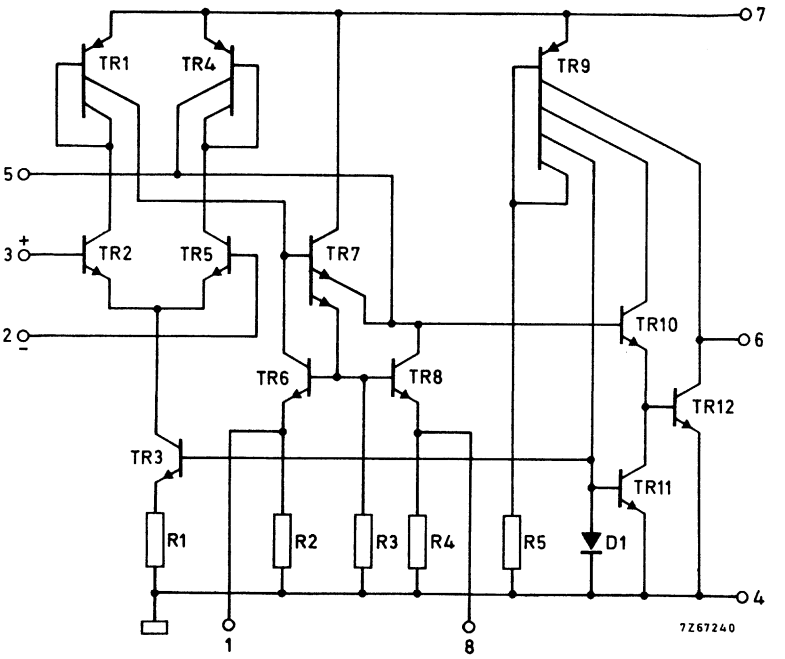
PACKAGE OUTLINE

Dimensions in mm

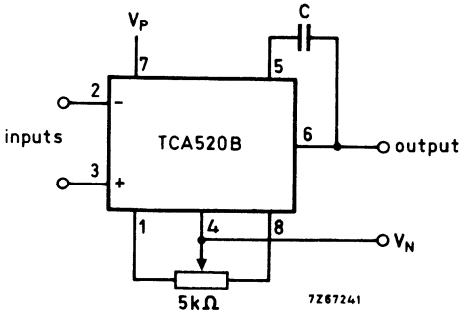
8 lead plastic dual in-line



CIRCUIT DIAGRAM



CONNECTION DIAGRAM AND PINNING



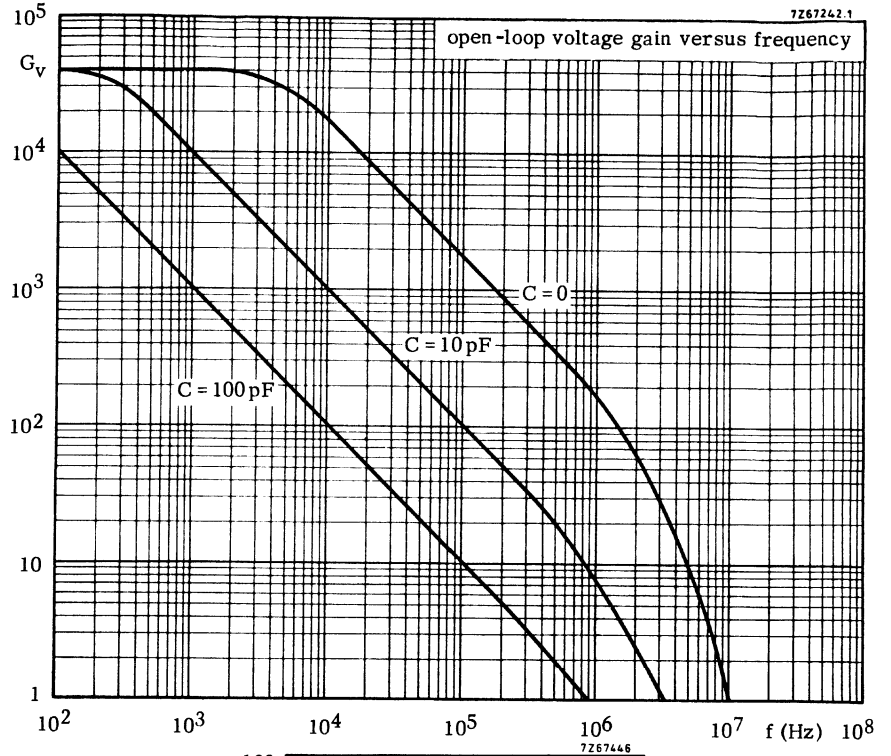
1. Balance
2. Inverting input
3. Non -inverting input
4. Negative supply (V_N)
5. Frequency compensation
6. Output
7. Positive supply (Vp)
8. Balance

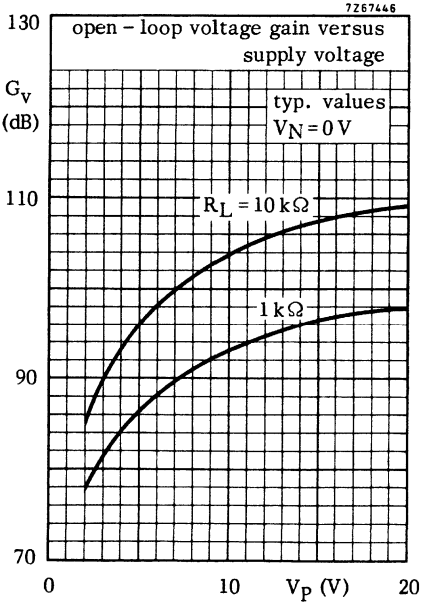
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

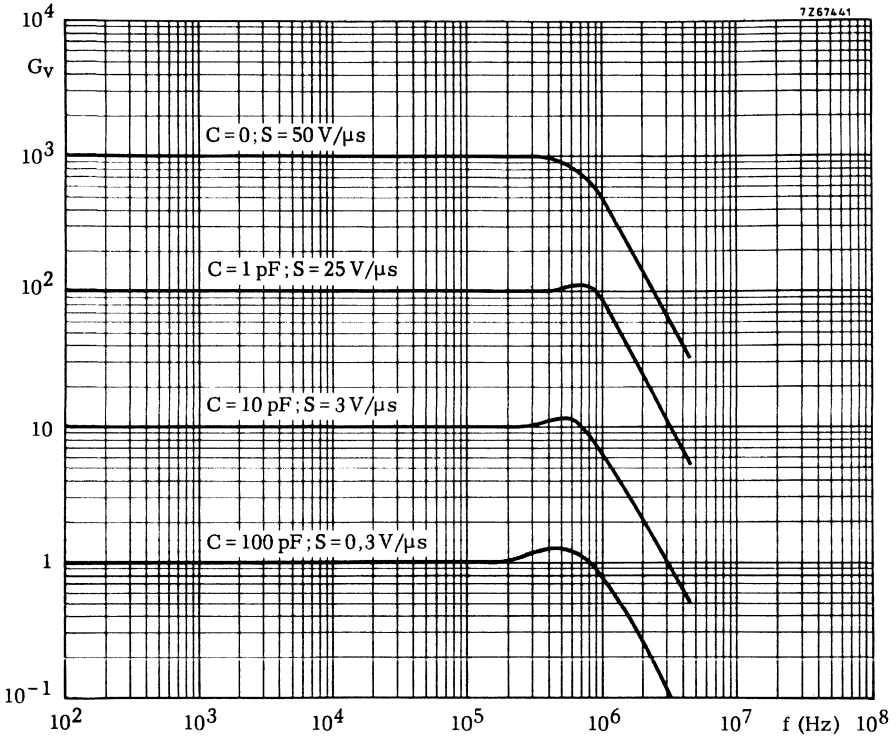
Voltages			
Positive supply voltage	V_P	max.	11 V
Negative supply voltage	V_N	max.	11 V
Differential input voltage	$\pm V_{2-3}$	max.	6 V
Power dissipation	P_{tot}	max.	310 mW
Temperatures			
Operating ambient temperature	T_{amb}		−25 to +70 °C
Storage temperature	T_{stg}		−55 to +125 °C

CHARACTERISTICS V_P = 5 V; V_N = 0 V; T_{amb} = 25 °C; R_L connected between output (pin 6) and positive supply (pin 7).

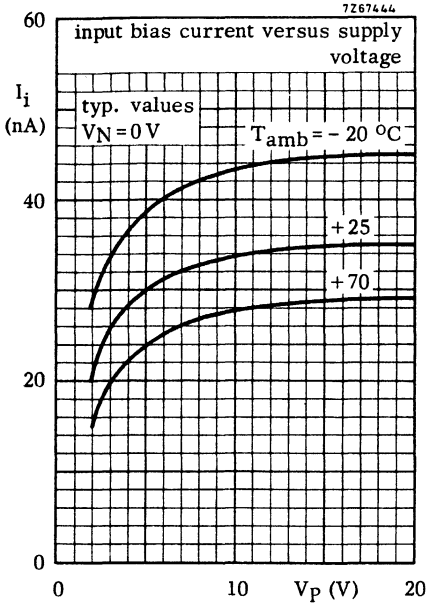
Voltage gain at R_L = 5 kΩ	G_v	typ.	40 000
Input offset voltage	V_{io}	typ.	2 mV
		<	6 mV
Input bias current	I_i	typ.	30 nA
		<	100 nA
Input offset current	I_{io}	typ.	5 nA
		<	30 nA
Input voltage range	V_i	>	V_N + 0,9 V to V_P − 0,5 V
Peak output voltage range at R_L = 5 kΩ	V_{OM}	>	V_N + 0,1 V to V_P − 0,1 V
Output sink current at $V_O = V_N + 0,4$ V	I_{sink}	typ.	12 mA
Output source current at $V_O < V_P - 0,4$ V	I_{source}	typ.	0,2 mA
Power dissipation at I_O = 0	P_{tot}	typ.	5 mW
Total supply current	I_{tot}	typ.	1 mA
Slew rate (unity gain) at R_L = 1 kΩ; C = 100 pF	S	typ.	0,3 V/us
at R_L = 1 kΩ; C = 0 pF	S	typ.	50 V/us

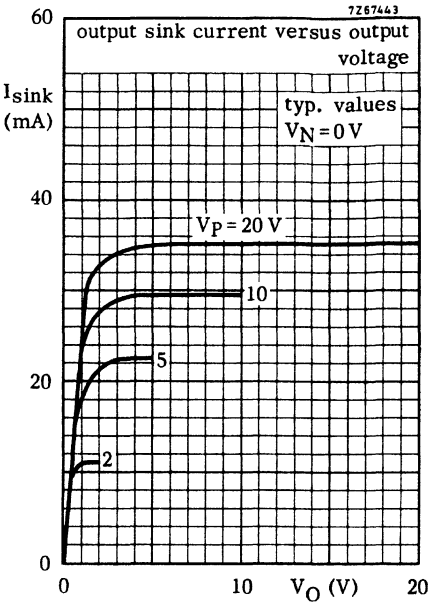

7Z67242.1
open-loop voltage gain versus frequency
10^5
G_v
10^4
10^3
10^2
10
1
C = 0
C = 10 pF
C = 100 pF
10^2
10^3
10^4
10^5
10^6
10^7
f (Hz)
10^8

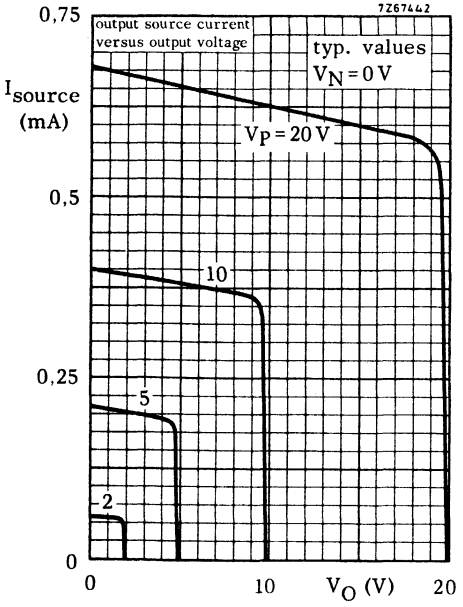

7Z67446
130
open – loop voltage gain versus supply voltage
G_v (dB)
typ. values
V_N = 0 V
110
R_L = 10 kΩ
1 kΩ
90
70
0
10
V_P (V)
20

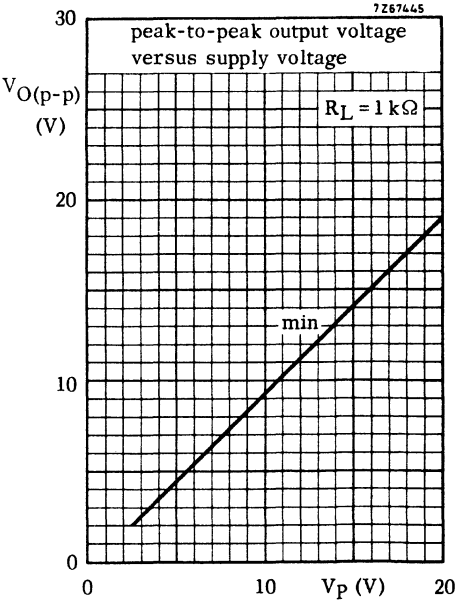


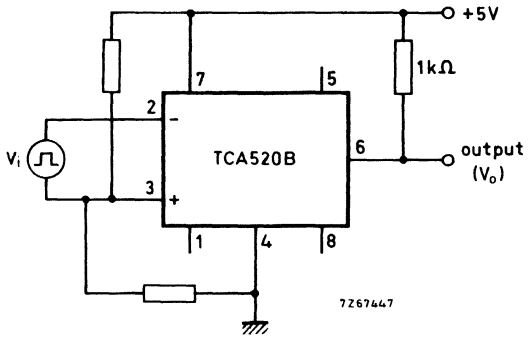
Frequency response and slew-rate for various closed-loop gains

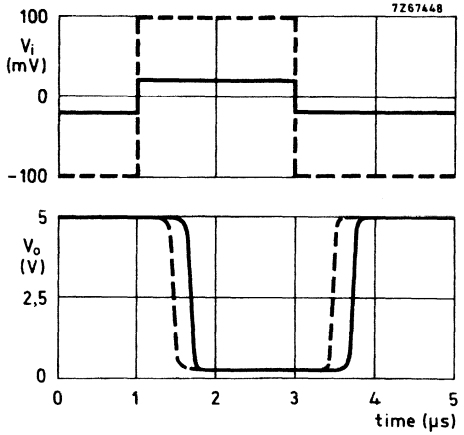

7Z67444
input bias current versus supply voltage
typ. values
$V_N = 0$ V
$T_{amb} = -20$ °C
+25
+70
I_i (nA)
60
40
20
0
0
10
V_P (V)
20


7Z67443
output sink current versus output voltage
typ. values
$V_N = 0$ V
$V_P = 20$ V
10
5
2
I_{sink} (mA)
60
40
20
0
0
10
V_O (V)
20


7Z67442
output source current versus output voltage
typ. values
$V_N = 0$ V
$V_P = 20$ V
10
5
2
I_{source} (mA)
0,75
0,5
0,25
0
0
10
V_O (V)
20


7Z67445
peak-to-peak output voltage versus supply voltage
$R_L = 1$ kΩ
min
$V_{O(p-p)}$ (V)
30
20
10
0
0
10
V_P (V)
20





The TCA520B used as comparator; pulse delays when the circuit is 20 or 100 mV overdriven.

SYNCHRONOUS DEMODULATOR FOR TV RECEIVERS

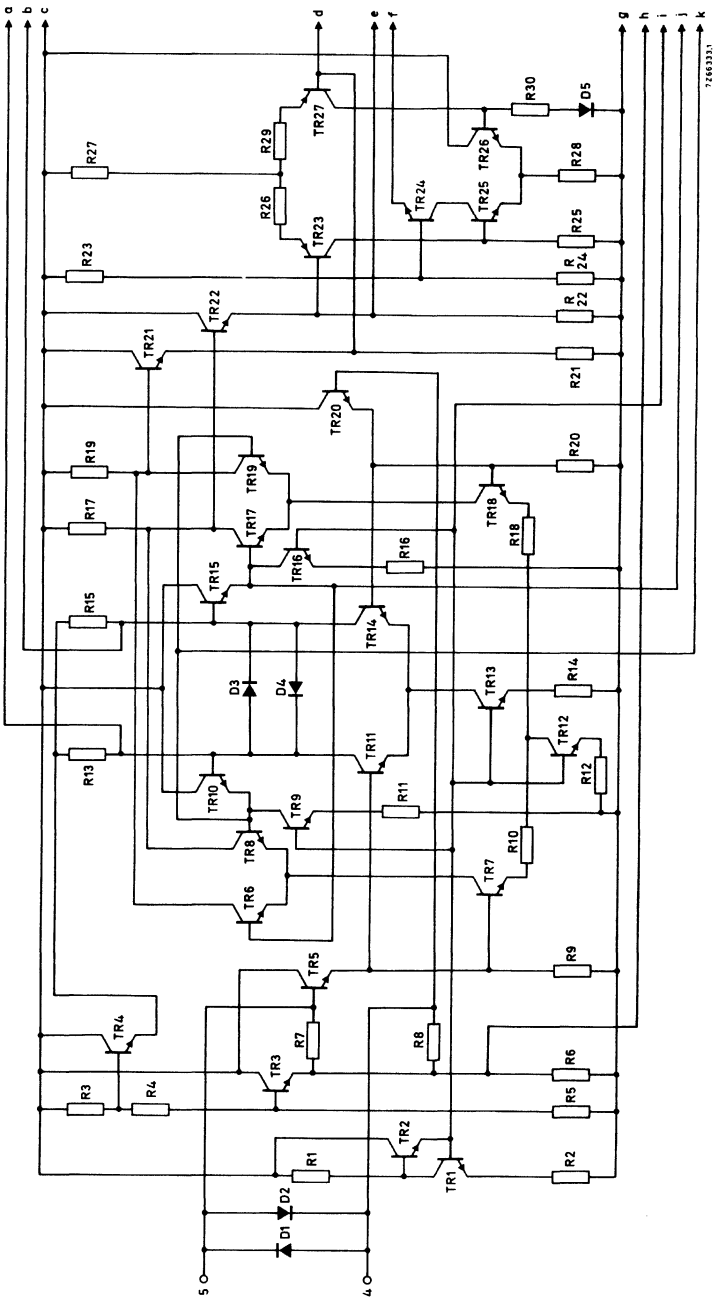
The TCA540 is a silicon monolithic integrated synchronous demodulator for television receivers which combines the following functions:

- synchronous demodulator with passive regeneration of the reference carrier
- white spot inverter (inverts white spots, which can occur because of the principle of synchronous demodulation).
- video pre-amplifier
- a.f.c. circuit

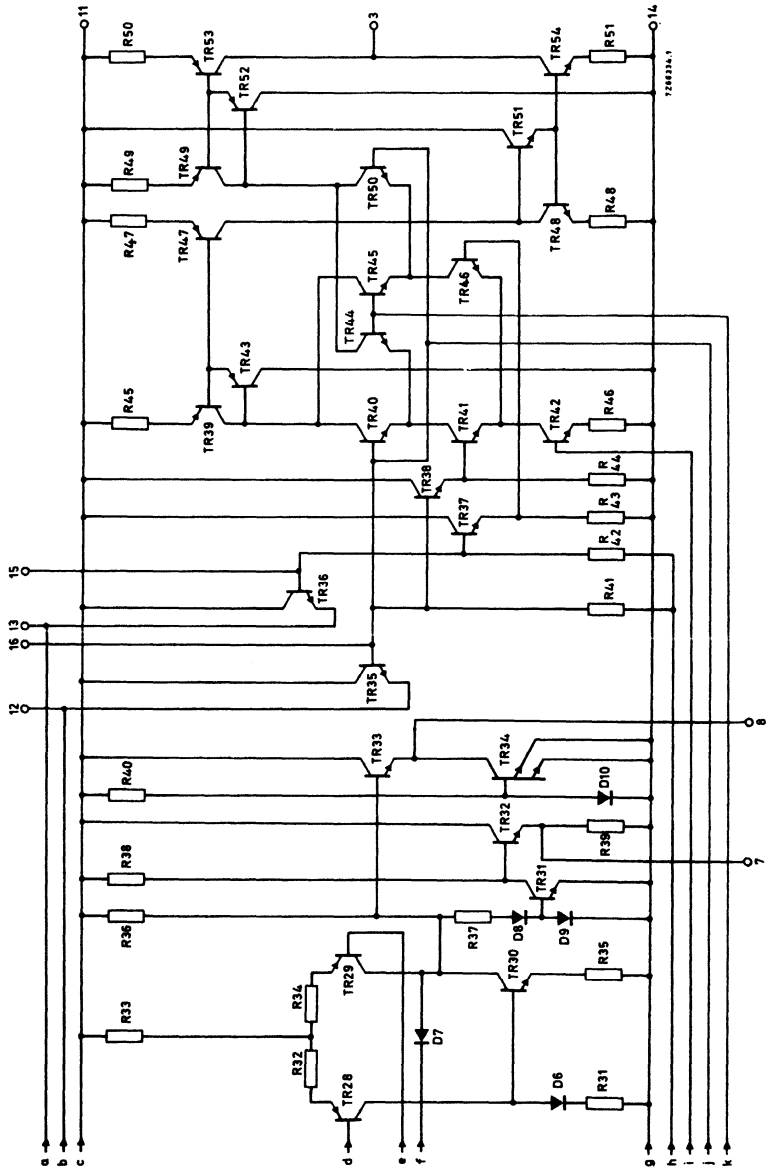
QUICK REFERENCE DATA				
Supply voltage	V_{11-14}	nom.	12	V
Supply current	I_{11}	typ.	40	mA
Input voltage (r.m.s. value) for 3 V peak-to-peak output voltage	$V_{4-5(rms)}$	typ.	70	mV
Differential gain (at pin 8)	dG	typ.	2	%
Differential phase (at pin 8)	$d\varphi$	typ.	2^o	
A.F.C. output voltage	V_{3-14}		1 to 11	V
A.F.C. sensitivity per kHz (R_L = 50 kΩ)	V_{3-14}	typ.	40	mV

PACKAGE OUTLINE TCA540 : 16 lead plastic dual in-line (type A) (See General Section)
TCA540Q: 16 lead plastic quadruple in-line (See General Section)

CIRCUIT DIAGRAM



CIRCUIT DIAGRAM (continued)



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	V_{11-14}	max.	18	V [1]
Temperatures				
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		−25 to +55	°C

CHARACTERISTICS

Supply voltage range (pin 11)	V_{11-14}		10,2 to 13,2	V
Supply current	I_{11}	typ.	40	mA

The following characteristics are measured at T_{amb} = 25 °C; V_{11-14} = 12 V; f_o = 38,9 MHz unless otherwise specified.

Demodulator circuit

Zero signal d.c. outputs	V_{7-14}	typ.	5,7	V
	V_{8-14}	typ.	6	V
Input voltage (r.m.s. value) for 3 V peak-to-peak output voltage	V_{4-5}	typ.	70	mV [2]
Input resistance	R_{4-5}	typ.	6	kΩ
Input capacitance	C_{4-5}	typ.	4,7	pF
Bandwidth of video output (3 dB; pin 8)	B	typ.	5	MHz
Output resistances	R_{8-14}	typ.	35	Ω
	R_{7-14}	typ.	75	Ω
Differential gain (pin 8) D.S.B.	dG	typ.	2	%
S.S.B.	dG	typ.	5	%
Differential phase (pin 8) D.S.B.	$d\varphi$	typ.	2	°
S.S.B.	$d\varphi$	typ.	3	°

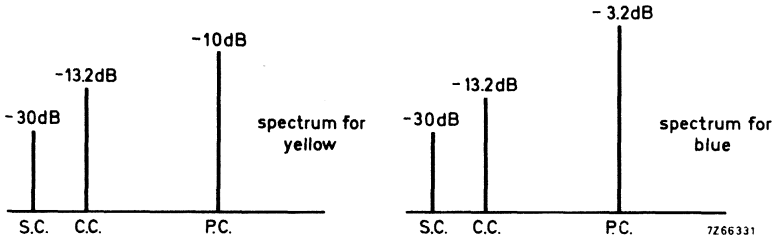
1) Allowed only while receiver is warming up.
2) Input signal modulated in accordance with the CCIR standard system B.

CHARACTERISTICS (continued)

Intermodulation (see input conditions below)

Blue spectrum (pin 8)	typ.	60	dB
Yellow spectrum (pin 8)	typ.	52	dB

Input conditions for intermodulation measurements (75% saturation):



S.C. : sound carrier attenuation
C.C. : chrominance carrier attenuation
P.C. : picture carrier attenuation

} with respect to top sync level

The sound-chrominance beat suppression is related to the B.W. amplitude with a top sync level of 3 V.

A.F.C. circuit (see figures 1 and 2 on pages 8 and 9)

Output control voltage	V_{3-14}		1 to 11	V
Sensitivity per kHz (R_L = 50 kΩ)	V_{3-14}	typ.	40	mV

PINNING

1. Not connected
2. Not connected
3. A.F.C. output
4. Balanced i.f. input
5. Balanced i.f. input
6. Not connected
7. Video output (pos. going sync)
8. Video output (neg. going sync)
9. Not connected
10. Not connected
11. Supply voltage (positive)
12. Tank coil connection (reference carrier)
13. Tank coil connection (reference carrier)
14. Earth (negative supply)
15. Tank coil connection (a.f.c.)
16. Tank coil connection (a.f.c.)

APPLICATION INFORMATION

Below some information is given about the external circuit.
The function is quoted against the corresponding pin numbers.

1. Not connected
2. Not connected
3. A.F.C. output

This output is a current source, so for driving the tuner the current must be translated into a voltage and this has been done by means of a network as shown in figure 3 on page 9. The network load is about 50 kΩ.
With this load, a sensitivity is obtained of about 40 mV/kHz.
Since a.f.c. is most important at u.h.f., the control network has been designed for optimum holding range and correction factor in this band, combined with the ELC2000S tuner.
The holding range with this control network is limited to about 6 MHz for u.h.f., so in this case it is not necessary to switch off the a.f.c. during tuning.
The correction factor ranges from 3,3 for v.h.f. to more than 20 in the u.h.f. band.
The table below gives examples for some channels in an application using the ELC2000S.

channel	catching range (MHz)	holding range (MHz)	correction factor
4	−0,6 to +0,5	−0,6 to +0,5	3,3
9	−0,8 to +0,8	−0,8 to +0,8	5
28	−2,8 to +0,9	−2,8 to +2,8	18
60	−2,3 to +0,7	−2,3 to +2,3	14

APPLICATION INFORMATION (continued)

4. Balanced i.f. input (in conjunction with pin 5)

   A balanced input is provided at pins 4 and 5. The d.c. level is set internally, and the signal should be applied from a floating transformer winding or through coupling capacitors. An unbalanced signal may be applied to either pin, the other has to be decoupled to earth by a capacitor of about 1,5 nF. The input impedance is typically 6 kΩ/4, 7pF. The input signal for 3 V peak-to-peak output signal is about 70 mV (rms).

5. Balanced i.f. input (see pin 4).

6. Not connected

7. Video output (positive going sync)

   The a.c. performance of this output is the same as that of pin 8. The d.c. level has a spread of ±10%.

8. Video output (negative going sync)

   This video signal is intended to be used for driving the video output stage in a black-and-white receiver or the luminance channel in a colour receiver. The signal has excellent figures for differential gain and phase so that also chroma and sound take-off is possible at this output.
   This output is matched with the TBA890 or TBA900 signal processing integrated circuit (see figure 1 on page 8).
   For use with the TBA500 (luminance combination) an external matching network is required (see figure 2 on page 9).
   A 5,5 MHz trap can be connected in series with the video output for driving the luminance channel, to avoid sound-chroma beat in the video part of the receiver.
   This type of demodulator will cause white peaks in the video signal when interferences are received. For this reason a white spot inverter is used which detects white peaks and reverses them to black level.
   The zero signal d.c. level is 6 V ±5%.

9. Not connected

10. Not connected

11. Positive supply (12 V)

    Correct operation is obtained at voltages between 10,2 V and 13,2 V.
    During short periods (e.g. while tubes are warming up) a supply voltage of 18 V is allowed.

12. Reference tuned circuit (in conjunction with pin 13)

    A tuned circuit is connected between pins 12 and 13 to provide the carrier filtering. The damping impedance between these two pins is about 6 kΩ. The choice of the L/C ratio of the tuned circuit is a compromise between a good figure for differential gain and intermodulation products. Excellent differential gain/phase performance requires a low tuning capacitance. However, the lowest intermodulation products will be obtained by a large tuning capacitance. A proved practical value of 47 pF gives good results. The unloaded quality factor in this circuit has to be >50.

13. Reference tuned circuit (see pin 12)

APPLICATION INFORMATION (continued)

14. Negative supply (earth)

15. A.F.C. tuned circuit (in conjunction with pin 16)

    This circuit is loosely coupled to the reference tuned circuit of the demodulator by means of the collector-base capacitances of TR35 and TR36 (see circuit diagrams on pages 2 and 3). The unloaded quality factor of this tuned circuit has to be >70.
    The temperature stability is important for the a.f.c. reference tuned cicuit. Using a miniature coil-former with powder iron core a good compensation is obtained with a NP0 temperature coefficient capacitor.
    The drift of the a.f.c. is typical +1 kHz/°C.

16. A.F.C. tuned circuit (see pin 15)

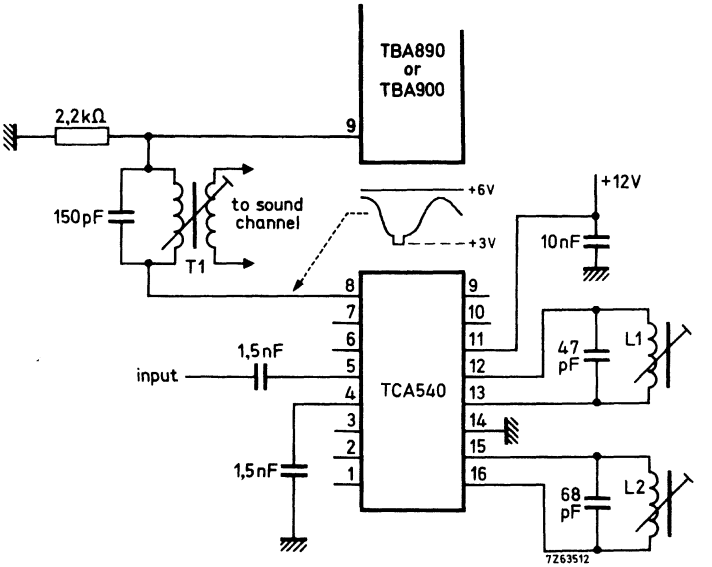
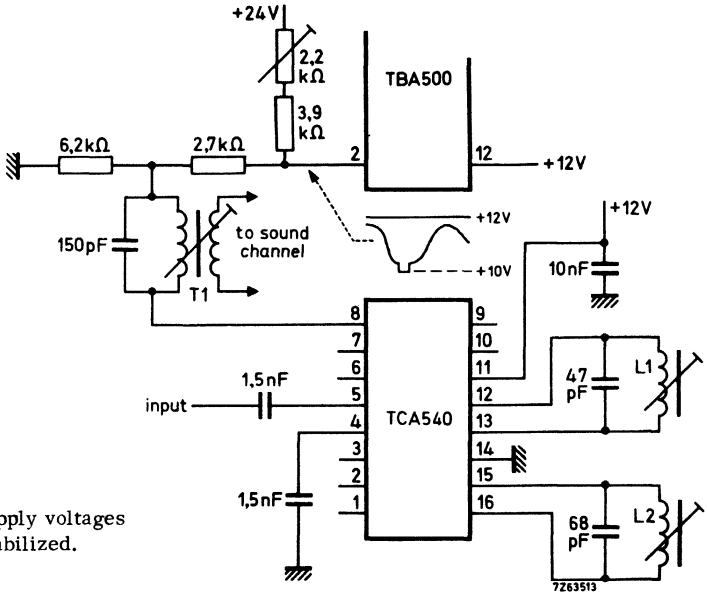


Fig. 1 Interface connections of the TCA540 with the TBA890 or TBA900

APPLICATION INFORMATION (continued)



Note: The two supply voltages must be stabilized.

Fig. 2 Interface connection of the TCA540 with the TBA500

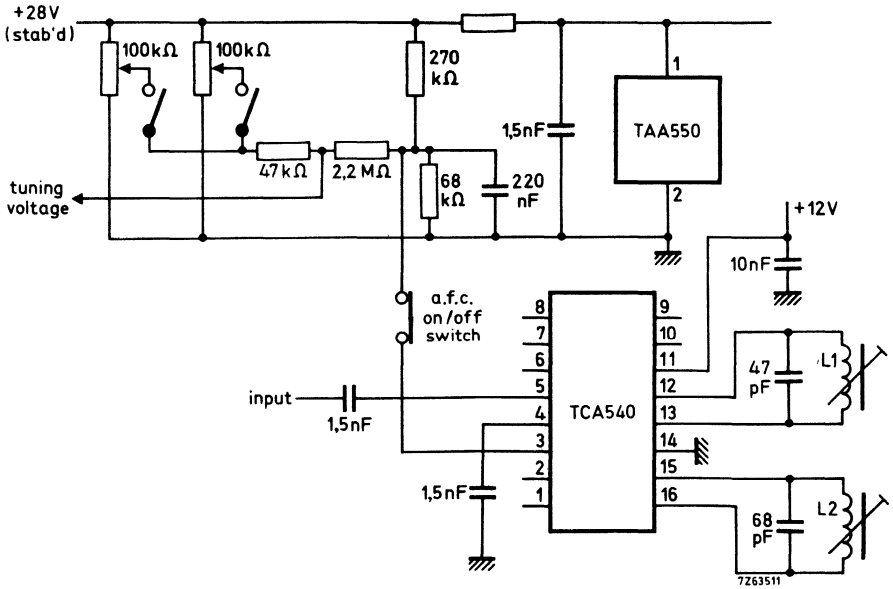


Fig. 3 A.F.C. with TCA540

INDEX OF TYPE NUMBERS

The inclusion of a type number in this publication does not necessarily imply its availibility.

OM200/S2	TAA970	TBA530Q	TBA720Q	TCA160	TCA540Q
SAJ110	TAB101	TBA540	TBA720A	TCA160B	
SAJ250A	TBA221	TBA540Q	TBA720AQ	TCA210	
SAJ250B	TBA221B	TBA550	TBA750A	TCA220	
TAA263	TBA221D	TBA550Q	TBA750AQ	TCA270	
TAA310	TBA222	TBA560B	TBA880	TCA270Q	
TAA310A	TBA281	TBA560BQ	TBA890	TCA290A	
TAA320	TBA480	TBA560C	TBA890Q	TCA410A	
TAA320A	TBA500N	TBA560CQ	TBA900	TCA410B	
TAA370	TBA500P	TBA570	TBA900Q	TCA420A	
TAA480	TBA510	TBA570Q	TBA915	TCA490A	
TAA550	TBA510Q	TBA673	TBA920	TCA490B	
TAA630S	TBA520	TBA690	TBA920Q	TCA490C	
TAA630T	TBA520Q	TBA700	TBA990	TCA520B	
TAA960	TBA530	TBA720	TBA990Q	TCA540	

MAINTENANCE TYPE LIST

The type numbers listed below are not included in this handbook.

Detailed information will be supplied on request.

TAA241	TAA350	TAA522	TAA630	TAD100
TAA242	TAA435	TAA560	TAA640	
TAA293	TAA450	TAA570	TAA700	
TAA300	TAA521	TAA580	TAA840	

741C → TBH 221
741 → TBA 222
723 → TBA 281

General

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